Course Code: ECE5005	**Course Title:** ADVANCED DIGITAL SYSTEM DESIGN **Type of Course: Theory (Program Core)**	**L- P- C**	3	0	3
Version No.	1.0				
Course Pre-requisites	Basic concepts of digital circuits like gates, flip-flops, registers, multiplexers, decoders etc.				
Anti-requisites	**NIL**				
Course Description	The focus of this course is to enable the students to Design the synchronous and Asynchronous Digital Systems through the study of ASM & FSM charts, Hardware description language coding, Reduction and assignments of state tables. Further, it elaborates the Test Generation and Fault diagnosis of Combinational circuits by conventional methods. It introduces various methods to analyze sequential circuits. Further it elaborated the circuit design using programmable devices. This course emphasizes Fault detection and diagnosis of Advanced digital electronic circuits.				
Course Objective	The objective of the course is to familiarize the learners with the concepts of ADVANCED DIGITAL SYSTEM DESIGN and attain **SKILL DEVELOPMENT** through **PARTICPATIVE LEARNING**				
Course Outcomes	On successful completion of the course the students shall be able to: CO1: Summarize the minimization theories of Sequential Machines. CO2: Discover the sequential circuit using programmable devices. CO3: Practice the techniques for fault modeling of digital systems. CO4: Illustrate the various Fault diagnosis algorithm				
Course Content:					
Module 1	**Minimization and Transformation of Sequential Machines:**	Assignment	Memory Recall based Quizzes	**10** *Sessions*	
The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.					
Module 2	**Advanced Digital Design and SM Charts:**	Assignment/ mini project	Memory Recall based Quizzes	**10** *Sessions*	
Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, shift and add multiplier, Binary divider. - State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.					
Module 3	**Fault Modeling**	Assignment/ mini project	Programing / simulation	**11** *Sessions*	
Logic Fault model – Fault detection & Redundancy Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.					
Module 4	**Fault diagnosis**	Assignment/ mini project	Programing / simulation	**11** *Sessions*	

REGISTRAR

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

Targeted Application & Tools that can be used:
This course is contributed for placement in data science companies, research & development work and also useful to know the existing & developing Artificial Intelligence.
Professionally Used Software: HDL (VHDL/ Verilog HDL)/ C++ / MatLab, Phython

Text Books:

1. N. N. Biswas, "*Logic Design Theory*", PHI, 2009. ISBN:9780135243985, 013524398X the University of Michigan- Prentice Hall
2. Zvi Kohavi , "*Switching and Finite Automata Theory*", TMH, 2nd Edition, 2005.
3. Norman Balabanian, Bradley Carlson, "*Digital Logic Design Principles*" Wiley Student Edition, 2007.

Reference Books

1. M. Abramovici, Melnin Breuer, Arthur Friedman, "*Digital System Testing and Testable Design*", Jaico Publications, Reprint Edition, 2008.
2. Charles H. Roth Jr., "*Fundamentals of Logic Design*", Cengage learning, 6th Edition, 2004.
3. Frederick. J. Hill & Peterson, "*Computer Aided Logic Design*", Wiley 4th Edition, 1993.

Online Resources (e-books, notes, ppts, video lectures etc)

1. State Minimization in synchronous sequential circuits - YouTube
2. Sequence detector 1100 || sequence detector 1101 overlapping mealy FSM - YouTube
3. **Ebook1:** Find PDF Logic Design Theory (colorado.edu)
4. **Ebook2:** Digital Systems Design | Download book (freebookcentre.net)
5. **Nptel** Digital System Design - Course (nptel.ac.in)
6. NPTEL :: Electrical Engineering - NOC:Digital System Design
7. **https://www.researchgate.net/publication/348235247_Advanced_Digital_System_Design_-_A_Practical_Guide_to_Verilog_Based_FPGA_and_ASIC_Implementation/link/5ff4764d92851c13feefa0d2/download**
8. **https://www.researchgate.net/publication/3897013_Fault_Equivalence_Identification_Using_Redundancy_Information_and_Static_and_Dynamic_Extraction**
9. **http://www.pld.ttu.ee/diagnostika/theory/fault.html**

Topics relevant to "Skill development": Machine Minimization
For developing **Skill development"** through **Participative Learning techniques**. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. G MUTHUPANDI
Recommended by the Board of Studies on	**BOS NO: 15th BOS held on 28/07/2022**
Date of Approval by the Academic Council	**Academic Council Meeting No. 18, Dated 3/08/2022**

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

A-2 [2022] COURSE HAND OUT

SCHOOL	**:** SOE
DEPT.	**:** ECE
DATE OF ISSUE	**: 27/08/2022**
NAME OF THE PROGRAM	**:** M. Tech
P.R.C. APPROVAL REF.	**: PU/AC-18.4/ECE15/ESV/2022-24**
SEMESTER/YEAR	**: 1**
COURSE TITLE & CODE	**: ADVANCED DIGITAL SYSTEM DESIGN** & ECE5005
COURSE CREDIT STRUCTURE	**:** 3-0-3
CONTACT HOURS	**:** 45
COURSE INSTRUCTORS	**: Dr. Muthupandi G**

PROGRAM OUTCOMES:

Graduates of the M. Tech. Program in Electronics and Communication Engineering will be able to:

PO1: An ability to analyze, manage and supervise engineering systems and processes with the aid of appropriate advanced tools.

PO2: An ability to design a system and process within constraints of health, safety, security, economics, manufacturability to meet desired needs.

PO3: An ability to carry out research in the respective discipline and publish the findings.

PO4: An ability to effectively communicate and transfer the knowledge/ skill to stakeholders.

PO5: An ability to realize the impact of engineering solutions in a contemporary, global, economical, environmental, and societal context for sustainable development.

COURSE PREREQUISITES:

Knowledge of C or Python Language, Knowledge of stm32 etc.,

COURSE DESCRIPTION:

REGISTRAR PRESIDENCY UNIVERSITY Registrar BANGALORE

The focus of this course is to enable the students to Design the synchronous and Asynchronous Digital Systems through the study of ASM & FSM charts, Hardware description language coding, Reduction and assignments of state tables. Further, it elaborates the Test Generation and Fault diagnosis of Combinational circuits by conventional methods. It introduces various methods to analyze sequential circuits. Further it elaborated the circuit design using programmable devices. This course emphasizes Fault detection and diagnosis of Advanced digital electronic circuits..

COURSE OBJECTIVES:

The objective of the course is to familiarize the learners with the concepts of **ADVANCED DIGITAL SYSTEM DESIGN** and attain **SKILL DEVELOPMENT** through **PARTICPATIVE LEARNING**

COURSE OUTCOMES:

On successful completion of the course the students shall be able to:

CO1: Summarize the minimization theories of Sequential Machines

CO2: Discover the sequential circuit using programmable devices.

CO3: Practice the techniques for fault modeling of digital systems.

CO4: Illustrate the various Fault diagnosis algorithm

MAPPING OF C.O. WITH P.O.

[H-HIGH, M- MODERATE, L-LOW]

CO N0.	PO 1	PO 2	PO 3	PO 4	PO 5
1	H	H	M	L	M
2	L	H	H	L	M
3	L	H	M	L	M
4	L	M	H	M	H

COURSE CONTENT (SYLLABUS):

Module: 1: Minimization and Transformation of Sequential Machines:: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards. **[10 hours] [Knowledge]**

Module: 2: Advanced Digital Design and SM Charts:: Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, shift and add multiplier, Binary divider. - State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.

[10 hours] [Comprehension]

Module 3: Fault Modeling: Logic Fault model – Fault detection & Redundancy Fault equivalence and fault location – Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.
[11 hours] [Comprehension]

Module 4: Fault Diagnosis: Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults. **[11 hours] [Comprehension]**

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

SKILL SETS TO BE DEVLOPED:

1. An attitude of enquiry.
2. Confidence and ability to tackle new problems.
3. Ability to interpret events and results.
4. Write reports.
5. The ability to follow standard /Legal procedures.
6. An awareness of the Professional Ethics.

DELIVERY PROCEDURE (PEDAGOGY): Lectures will be conducted with aid of Microsoft Teams. Assignments based on course contents will be given to the students at the end of each unit/topic and will be evaluated at regular interval.

SELF-LEARNING TOPICS: Kohavi algorithm, Test Pattern Generation, D – algorithm, PODEM Testable PLA design.

BLENDED LEARNING USING VIDEOS: PAL and PLA.

FLIPPED CLASS ROOM TOPIC: State machine reduction technique

PARTICIPATIVE LEARNING: How Optimization Algorithms are applicable for state reduction

REFERENCE MATERIALS: Textbooks, reference books, any other resources, like webpages.

(i) Text Books:

Text Books:

4. N. N. Biswas, "*Logic Design Theory*", PHI, 2009. ISBN:9780135243985, 013524398X
   the University of Michigan- Prentice Hall
5. Zvi Kohavi , "*Switching and Finite Automata Theory*", TMH, 2nd Edition, 2005.
6. Norman Balabanian, Bradley Carlson, "*Digital Logic Design Principles*" Wiley Student Edition, 2007

(ii) Reference book:

4. M. Abramovici, Melnin Breuer, Arthur Friedman, "*Digital System Testing and Testable Design*", Jaico Publications, Reprint Edition, 2008.
5. Charles H. Roth Jr., "*Fundamentals of Logic Design*", Cengage learning, 6th Edition, 2004.
6. Frederick. J. Hill & Peterson, "*Computer Aided Logic Design*", Wiley 4th Edition, 1993.

(iii) Class Notes:

(iv) E-content:

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

10. State Minimization in synchronous sequential circuits - YouTube
11. Sequence detector 1100 || sequence detector 1101 overlapping mealy FSM - YouTube
12. **Ebook1:** Find PDF Logic Design Theory (colorado.edu)
13. **Ebook2:** Digital Systems Design | Download book (freebookcentre.net)
14. **Nptel** Digital System Design - Course (nptel.ac.in)
15. NPTEL :: Electrical Engineering - NOC:Digital System Design
16. **https://www.researchgate.net/publication/348235247_Advanced_Digital_System_Design_-_A_Practical_Guide_to_Verilog_Based_FPGA_and_ASIC_Implementation/link/5ff4764d92851c13feefa0d2/download**
17. **https://www.researchgate.net/publication/3897013_Fault_Equivalence_Identification_Using_Redundancy_Information_and_Static_and_Dynamic_Extraction**
18. **http://www.pld.ttu.ee/diagnostika/theory/fault.html**

GUIDELINES TO STUDENTS:

Students have to attend classes regularly and follow the session very carefully. Here in handout we mentioned pre requisitions, go through the topics once. The students are directed to maintain separate note book to write important discussions/key points during the lecture

PRESIDENCY UNIVERSITY LIBRARY LINK: https://presiuniv.knimbus.com/user#/home

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

COURSE SCHEDULE:

Sl. No.	ACTIVITY	STARTING DATE	CONCLUDING DATE	TOTAL NUMBER OF PERIODS
1.	Over View of the course			01
2.	Module : 01			12
3.	Module 01 revision			1
4.	Assignment 1			---
5.	Module : 02			13
6.	Module 02 revision			1
7.	Mid Term Examination			NA
8.	Mid Term Paper Discussion			03
9.	Module:03			10
8	Group Discussion /Case Study			---
9	End Term Examination			NA
			TOTAL	41

SCHEDULE OF INSTRUCTION

Sl. No	Session No / Date*	Lesson Title	Topics	CO No	Delivery Mode	Reference
1.		Overview and integration	Introduction to Advanced digital design concepts and explanation of how they are related with Digital Electronics.	-NA-	Online Microsoft Teams	
2.			Characteristics of Digital Systems.	1		CN, R1
3.		The Finite State Model .	Capabilities and limitations of FSM	1		CN, R1
4.			State equivalence and machine minimization	1		CN, R1
5.			Simplification of incompletely specified machines	1		CN, R1
6.		FSM Design	Fundamental mode model	1		CN, T1
7.			Sequence detector FSM (Mealy overlapping and Non-overlapping)	2		CN, T1
8.			Sequence detector FSM (Moore non-overlapping and overlapping)	2		
9.			Flow table , State reduction – Minimal closed covers	2		
10.			Races, Cycles and Hazards.	2		T1 R1 CN

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

11.		**Advanced Digital Design**	Digital Design Using ROMs PALs and PLAs	4		T1 R1 CN
12.			BCD Adder, 32 – bit adder	4		T1 R1 CN
13.		**SM Charts:**	State graphs for control circuits	4		T1 R1 CN
14.			shift and add multiplier	4		T1 R1 CN
15.			Binary divider	4		T1 R1 CN
16.			State machine charts			T1 R1 CN
17.			Derivation of SM Charts	4		T1 R1 CN
18.			Realization of SM Chart	4		T1 R1 CN
19.			Implementation of Binary Multiplier	4		T1 R1 CN
20.			Mid Sem Exam Review	3		T1 R1 CN
21.			Mid Sem Exam Discussion	4		T1 R1 CN
22.		Logic Fault model	FAULT			
23.			Fault dominance	4		T1 R1 CN
24.			Single stuck at fault model			
25.			Multiple stuck at fault models			
26.			Bridging fault model			
27.			Course Project Progress Review			
28.			Course Project Progress Review			
29.		Fault Modelling	Fault Modeling & Test Pattern Generation: Logic Fault model	4		T1 R1 CN
30.			Fault detection & Redundancy Fault equivalence and fault location	4		T1 R1 CN
31.			Fault dominance – Single stuck at fault model – Multiple stuck at fault models–Bridging fault model.			
Completion of Module 3						
32.		Fault diagnosis	Fault diagnosis of combinational circuits by conventional methods	4		CN
33.			Path sensitization techniques.	4		CN
34.			Test algorithms	4		CN
35.			Examples for test patterns generation			
36.			Examples Continued			
37.			PODEM, Random testing			
38.			Transition count testing			
39.			Signature analysis and test bridging faults.			
40.						

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

Completion of Module 4						
41.	24/03/2021		Project Submission and Evaluation			
42.	26/03/2021		End Term Exam Review			

* These dates are only indicative - applicable to one section handled by subject IC. Dates will vary from section to section.

ASSESSMENT SCHEDULE:

Topics relevant to "Skill development": Machine Minimization
For developing **Skill development"** through **Participative Learning techniques**. This is attained through the Project as mentioned in the assessment component

Sl. No	**Assessment type**	**Contents**	**CO. NO**	**Duration In Minutes**	**Marks**	**Weightage**	**Venue, DATE &TIME**
1.	Mid Term	Module 1,2	CO1,CO2	90 min	60	30%	
2.	End term Examination	Module 1,2,3	CO1,CO2,CO3	180 min	100	50%	
3.	Mini Project	-	CO1,CO2,CO3	NA	20	10%	
4.	Assignment		CO1, CO2, CO3	NA	10	5%	
5.	Assignment-Review of digital / e-resources from Pres. Univ. link given in the References Section - (Mandatory to submit screenshot accessing digital resource. Otherwise it will not be evaluated)	https://doi.org/10.1016/j.procs.2021.01.171 https://doi.org/10.1016/j.micpro.2020.103782 https://doi.org/10.1016/j.micpro.2020.103725 https://doi.org/10.1016/j.neunet.2019.09.0	CO1,CO2,CO3	NA	10	5%	Will be announced one week prior to submission

REGISTRAR

		24.					

COURSE CLEARANCE CRITERIA: A minimum of 75% attendance is required to attend the end term exam. Make-up policy will be only as per academic regulation. There will be no make-up for ASSIGNMENT and QUIZ

Method of Assessment **for Courses with Credit Structure (L –T – 0) or (L – 0 – 0)**			
	Components of Continuous Assessments	**Weightage (% of Total Marks)**	**Duration of Assessment**
1.	Mid Term	30%	1.5 hour
2.	This Component of continuous assessment shall consist of at least TWO (02) of the following: (1) Group Discussion /Case Study (2) Assignment/Quiz	20%	NA
3.	End Term Final Examinations	50%	3 hours
	Total	**100%**	

MAKEUP POLICY:

If the student misses an evaluation component, he/she may be granted a make-up. In case of an absence that is foreseen, make-up request should be personally made to the Instructor-in-Charge, well ahead of the scheduled evaluation component. Reasons for unanticipated absence that qualify a student to apply for make-up include medical emergencies or personal exigencies. In such an event, the student should contact the Instructor-in-Charge as soon as practically possible.

CONTACT TIMINGS IN THE CHAMBER FOR ANY DISCUSSIONS: It will be announced in the class. Interested students may meet the Instructor In-charge during the Chamber Consultation Hour to clear doubts.

SAMPLE THOUGHT PROVOKING QUESTIONS:

SL NO	**QUESTION**	**MARKS**	**CO. NO.**	**BLOOM'S LEVEL**
1.	A digital system is to be designed in which the month of the year is given as input in four bit form. The month January is represented as '0000',	6	CO1	L2

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

	February '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider the excess numbers in the input beyond '1011' as don't care conditions for system of four variables (A, B, C, D). Design and implement the simplified logic using NAND Gates.			
2.	Explain and Sketch FSM for Keypad scanner and Encoder.	4	CO2	L3
3.	Discuss the internal and external design challenges faced by an design engineer while implementing a sequential design for a traffic system.	6	CO1	L2
4.	Design an 4 bit ALU in HDL environment. Integrate the functionalities and verify it.	12	CO1, CO2, CO4	L4

Target set for course Outcome attainment:

Sl. No	CO. No.	Course Outcomes	Target set for attainment in percentage
1	CO1	Summarize the minimization theories of Sequential Machines	50%
2	CO2	Discover the sequential circuit using programmable devices.	40%
3	CO3	Practice the techniques for fault modeling of digital systems.	50%
	CO4	Illustrate the various Fault diagnosis algorithm	50%

Signature of the course Instructor:

This course has been duly verified Approved by the D.A.C.

Signature of the Chairperson D.A.C.

Course Completion Remarks &Self-Assessment.[This has to be filled after the completion of the course]

[Please mention about the course coverage details w.r.t. the schedule prepared and implemented. Any specific suggestions to incorporate in the course content. Any Innovative practices followed and its experience. Any specific suggestions from the students about the content, Delivery, Evaluation etc.]

Sl.no.	Activity	Scheduled Completion Date	Actual Completion Date	Remarks

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

	As listed in the course Schedule			
1	Midterm Examination			
3	End term Examination			
4	Mini Project / Assignment			

Any specific suggestion/Observations on content/coverage/pedagogical methods used etc.:

Course Outcome Attainment:

Sl.no	C.O. No.	Course Outcomes	Target set for attainment in percentage	Actual C.O. Attainment In Percentage	Remarks on attainment &Measures to enhance the attainment
01	CO1	Summarize the minimization theories of Sequential Machines	50%		
02	CO2	Discover the sequential circuit using programmable devices.	40%		
03	CO3	Practice the techniques for fault modeling of digital systems.	50%		
04	CO4	Illustrate the various Fault diagnosis algorithm	50%		

Name and signature of the Faculty member:

D.A.C. observation and approval:

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

BLOOM'S TAXONOMY

Learning Outcomes Verbs at Each Bloom Taxonomy Level to be used for writing the course Outcomes.

Cognitive Level	Illustrative Verbs	Definitions
Knowledge	arrange, define, describe, duplicate, identify, label, list, match, memorize, name, order, outline, recognize, relate, recall, repeat, reproduce, select, state	remembering previously learned information
Comprehension	classify, convert, defend, discuss, distinguish, estimate, explain, express, extend, generalize, give example(s), identify, indicate, infer, locate, paraphrase, predict, recognize, rewrite, report, restate, review, select, summarize, translate	grasping the meaning of information
Application	apply, change, choose, compute, demonstrate, discover, dramatize, employ, illustrate, interpret, manipulate, modify, operate, practice, predict, prepare, produce, relate schedule, show, sketch, solve, use write	applying knowledge to actual situations
Analysis	analyze, appraise, breakdown, calculate, categorize, classify, compare, contrast, criticize, derive, diagram, differentiate, discriminate, distinguish, examine, experiment, identify, illustrate, infer, interpret, model, outline, point out, question, relate, select, separate, subdivide, test	breaking down objects or ideas into simpler parts and seeing how the parts relate and are organized
Synthesis	arrange, assemble, categorize, collect, combine, comply, compose, construct, create, design, develop, devise, explain, formulate, generate, plan, prepare, propose, rearrange, reconstruct, relate, reorganize, revise, rewrite, set up, summarize, synthesize, tell, write	rearranging component ideas into a new whole
Evaluation	appraise, argue, assess, attach, choose, compare, conclude, contrast, defend, describe, discriminate, estimate, evaluate, explain, judge, justify, interpret, relate, predict, rate, select, summarize, support, value	making judgments based on internal evidence or external criteria

SCHOOL of ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Year: 2022-2023 (ODD) **Semester: M.Tech.,(ESV)** **Section:**

Course Title : Advanced Digital System Design.

Course Code : ECE5005

Type of Skill : Skill Development

Type of Activity : Participative Learning

Instructor in Charge : **Dr. Muthupandi G**.

Instructor for Section : Dr. Muthupandi G

Details about the activity : Students were asked to present on any

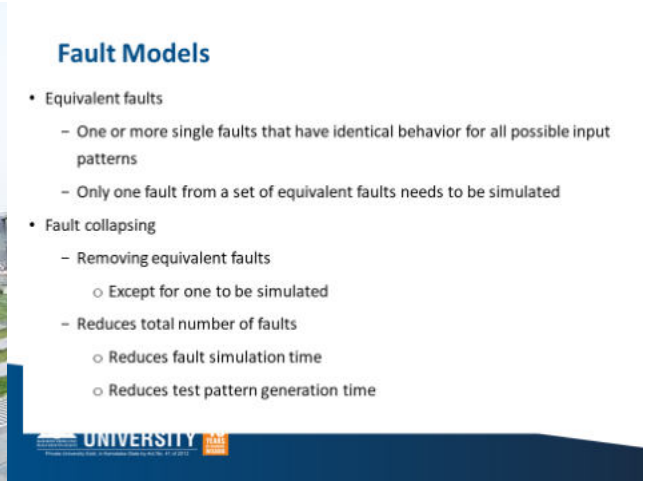
Mode of Activity : Presentation on Fault Models

Details of the students involved in the activity:

S.No	Name of the Student	Roll Number
1	CHARAGUDI DHANYA	20222ESV0001
2	SETTY REDDY VIGNESH	20222ESV0002

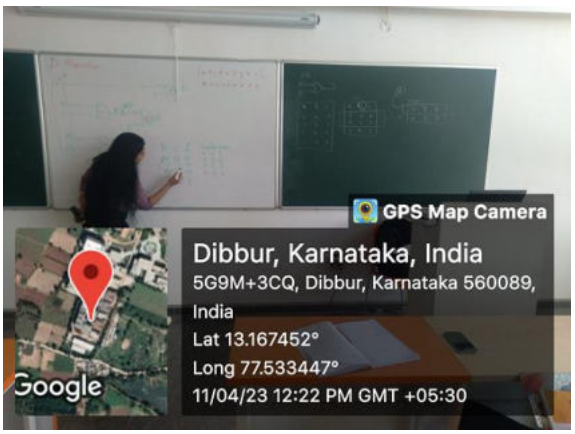
Date of presentation: 11.4.23 & 12.4.23

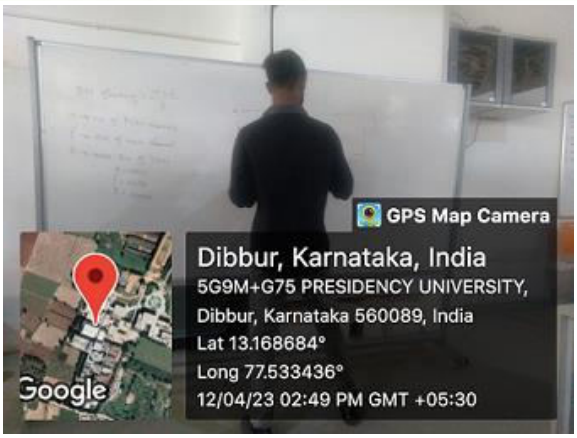
A fault model identifies targets for testing. Drastically reduces the number of faults. Makes analysis possible. Effectiveness measurable by experiments.



REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE





Remarks:

- By **participating in this presentation**, students were **learned** about the Fault Models Descriptions.
- This learning will **Develop their Skills** in Identify the fault in any machines

Signature of Instructor:

Signature of Instructor In-Charge :

HOD - ECE

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

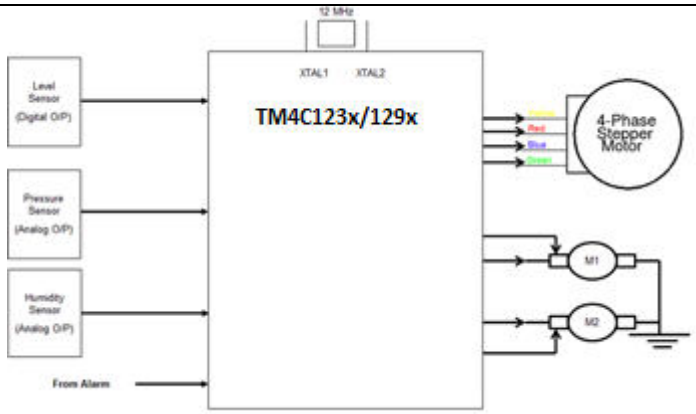
Course Code: ECE5008	**Course Title: Software for Embedded System** **Type of Course: Program Core Theory**	**L-P-C**	3	0	3
Version No.	1.0				
Course Pre-requisites	**Before attempting this course the student should have prior knowledge of Digital Logic and Operators, Some understanding of Microprocessors and/or Microcontrollers, Assembly Language Programming of any Microprocessors and/or Microcontrollers, Prior C Programming knowledge (would be an added advantage but not compulsory).**				
Anti-requisites	**NIL**				
Course Description	**This course focuses on the development of software for real-world embedded systems. Students will be exposed to various techniques for writing efficient codes for embedded products.** **The course will begin by giving an overview of controlling hardware systems using C programming language. In the next level use of Integrated Development Environment (IDE) tools will be undertaken for building and managing efficient programs and design. Installation of software tools as well as virtual machines, controlling of hardware kits etc. will be the key elements. To augment the learning process for independent software development students will be trained in compilation and make process by using various open-source compilers and tools such as GNU toolchain GNU, Git version control, Linux, Virtual Machines etc. Additionally, concepts like memory management, device driver development, compilers and debuggers, timers and interrupt systems, interfacing of devices, communications and networking in embedded systems will make students ready for industry.**				
Course Objective	**The objective of the course is to familiarize the learners with the software for embedded systems and attain SKILL DEVELOPMENT through PARTICPATIVE LEARNING**				
Course Outcomes	**On successful completion of this course the students shall be able to:** 1. Summarize the concepts to develop software for real time embedded systems. 2. Write efficient programs with IDE tools for embedded systems. 3. Demonstrate various programming steps using open-source compilers and tools for embedded software development. 4. Explain various concepts of memory management, device drivers, timers and interrupt systems, interfacing of devices, communications and networking in embedded systems.				
Course Content:					
Module 1	**Introduction to Embedded Systems Software Development**	Quiz	Memory Recall based Quizzes	**7 session**	
Topics: Review of Embedded Systems and Application Areas, Fundamentals of Software Engineering and Development Processes, Embedded Software - Safety, Security and Quality, Introduction to Embedded Software Modelling, Context Diagrams, State Charts / Finite State Machines (FSMs),.					

REGISTRAR

Module 2	**C-Programming for Embedded Systems**	Assignment / Quiz	Programming	**8 session**
Topics: Review of modeling languages for Embedded Software development, C-Programming Review, Programming ARM Controllers using C – Conditional Statements, Loop Statements, debugging, single stepping, breakpoints, pointers and data structures, variables, numbers and parameter passing.				
Module 3	**Memory Management and Device Driver Concepts**	Assignment	Analysis and Verification	**17 session**
Topics: Introduction to Memory Organization, Memory Architectures, Memory Segments, Data Memory, Special Keywords (Const, Extern & Static), The Stack, The Heap, Code Memory, Practice on Memory Manipulation Software, Incorporate Memory Manipulation Software into the build system and Evaluation of some Test Functions. Linux - Scripting and Configuration, Kernel Building, Building Libraries and Utilities, Generic Device Driver Development Concepts, Linux Device Drivers.				
Project Work/Assignment:				
1.Case Studies: At the end of the course students will be given 'real-world' application-based circuits like traffic light controller, LCD display, DC motor etc. as a case study. Students will be submitting a report which will include Circuit Diagrams, Design, Working Mechanism and Results etc. in appropriate format. **2. Book/Article review: At the end of each module a book reference or an article topic will be given to an individual or a group of students. They need to refer to the library resources and write a report on their understanding about the assigned article in an appropriate format. Presidency University Library Link .** **3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.** **4. Project Assignment: (Don't be specific)** **Assignment 1:** Recently there have been lot of controversies over use of Electronic Voting Machine (EVM) Systems in elections. You have been asked to design an "EVM System" to be used in elections. The system will have additional facility to webcast the voting process live to a central station using Wi-Fi/3G/4G connection by using a high-resolution camera and/or tablet (as of now avoid VVPAT facility). Draw a FSM diagram considering various states, inputs and Outputs. **Assignment 2:** Consider the figure shown below showing the layout of an Embedded System to be designed using the TM4C123x/129x microcontroller. Write a device driver for the individual modules shown such as for stepper motor control, dc motor control, timer and sensing inputs both digital as well as analog.				

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE



Text Book(s):

1. Joseph Yiu, "*The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors*," 3rd Edition, Newnes.

Reference(s):

Reference Book(s):

1. Michael Barr and Anthony Massa, "*Programming Embedded Systems with C and GNU Development Tools*," O'Reilly.
2. Haring D.D. et al., "Embedded Software Development With C," Springer.
3. Jane W S Liu, "Real – Time Systems", Prentice Hall, 2000.
4. Class Notes (CN).

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Video lectures on "Embedded System using Arm" by Prof. Dr.Indranil Sen Gupta, IIT KGP Lecture 01: Introduction to Embedded Systems - YouTube
2. Lecture series on Embedded Systems by Dr.Santanu Chaudhury,Dept. of Electrical Engineering, IIT Delhi . For more details on NPTEL visit http://nptel.ac.in

E-content:

1. Camposano, R., & Wilberg, J. (1996). Embedded system design. *Design Automation for Embedded Systems*, *1*(1), 5-50. Embedded system design | SpringerLink
2. Ryu, S., & Kim, S. C. (2020). Embedded identification of surface based on multirate sensor fusion with deep neural network. *IEEE embedded systems letters*, *13*(2), 49-52. Embedded Identification of Surface Based on Multirate Sensor Fusion With Deep Neural Network | IEEE Journals & Magazine | IEEE Xplore

Topics relevant to "SKILL DEVELOPMENT": Introduction to Embedded Systems, C-Programming for Embedded Systems. Memory management concepts for C programming for Skill Development through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Mrs. Aruna Dore
Recommended by the Board of Studies on	15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Meeting No. 18th , Dated 03/08/2022

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

PRESIDENCY UNIVERSITY

(Established under the Presidency University Act, 2013 of the Karnataka Act 41 of 2013)

ACA-2[2021] COURSE HAND OUT

SCHOOL: SOE **DEPT.: ECE** **DATE OF ISSUE: 27/08/2022**

NAME OF THE PROGRAM **:** M. Tech. Embedded System and VLSI

P.R.C. APPROVAL REF. **:** PU/AC-18.4/ECE15/ESV/2022-24

SEMESTER/YEAR **: 1**

COURSE TITLE & CODE **:** Software for Embedded Systems (ECE 5009)

COURSE CREDIT STRUCTURE **:** 3-0-0-3

CONTACT HOURS **: 45**

COURSE INSTRUCTOR **: Dr. Joseph Anthony Pratap**

PROGRAM OUTCOMES : Bolded outcomes are met by this course. Others are not met.

Graduates of the M. Tech. Program in Embedded System and VLSI will have the following abilities:

PO1. An ability to apply knowledge of mathematics, science and engineering in practice.

PO2. An ability to identify, critically analyze, formulate and solve engineering problems with comprehensive knowledge in the area of specialization.

PO3. An ability to select modern engineering tools and techniques and use them with dexterity.

PO4. An ability to design a system and process to meet desired needs within realistic constraints such as health, safety, security and manufacturability.

PO5. An ability to contribute by research and innovation to solve engineering problems.

PO6. An ability to devise and conduct experiments, interpret data and provide well-informed conclusions.

PO7. An ability to understand the impact of engineering solutions in a contemporary, global, economic, environmental, and societal context for sustainable development.

PO8. An ability to function professionally with ethical responsibility as an individual as well as in multidisciplinary teams with a positive attitude.

PO9. An ability to communicate effectively.

PO10. An ability to appreciate the importance of goal setting and to recognize the need for life-long reflective learning.

COURSE PREREQUISITES:

REGISTRAR

Before attempting this course the student should have prior knowledge of Digital Logic and Operators, Some understanding of Microprocessors and/or Microcontrollers, Assembly Language Programming of any Microprocessors and/or Microcontrollers, Prior C Programming knowledge (would be an added advantage but not compulsory).

COURSE DESCRIPTION:

This course focuses on the development of software for real-world embedded systems. Students will be exposed to various techniques for writing efficient codes for embedded products.
The course will begin by giving an overview of controlling hardware systems using C programming language. In the next level use of Integrated Development Environment (IDE) tools will be undertaken for building and managing efficient programs and design. Installation of software tools as well as virtual machines, controlling of hardware kits etc. will be the key elements. To augment the learning process for independent software development students will be trained in compilation and make process by using various open-source compilers and tools such as GNU toolchain GNU, Git version control, Linux, Virtual Machines etc. Additionally, concepts like memory management, device driver development, compilers and debuggers, timers and interrupt systems, interfacing of devices, communications and networking in embedded systems will make students ready for industry.

COURSE OBJECTIVE

The objective of the course is to familiarize the learners with the software for embedded systems and attain SKILL DEVELOPMENT through PARTICPATIVE LEARNING.

COURSE OUTCOMES:

On successful completion of the course the students shall be able to

5. Summarize the concepts to develop software for real time embedded systems.
6. Write efficient programs with IDE tools for embedded systems.
7. Demonstrate various programming steps using open-source compilers and tools for embedded software development.
8. Explain various concepts of memory management, device drivers, timers and interrupt systems, interfacing of devices, communications and networking in embedded systems.

MAPPING OF C.O. WITH P.O.

[H-HIGH , M- MODERATE, L-LOW]

CO. NO.	PO1	PO2	PO3	PO6	PO8	PO9
1.	L	L	L			L
2.	M	M	L	L	L	L
3.	M	M	M	M	L	L
4.	H	H	H	H	M	L

COURSE CONTENT (SYLLABUS):

Module 1: Introduction to Embedded Systems Software Development: Review of Embedded Systems and Application Areas, Fundamentals of Software Engineering and Development Processes, Embedded Software - Safety, Security and Quality, Introduction to Embedded Software Modeling, Context Diagrams, State Charts / Finite State Machines (FSMs),. **(7 Hrs) [Blooms level selected: Comprehension Level]**

Module 2: C-Programming for Embedded Systems: Review of modelling languages for Embedded Software development, C-Programming Review, Programming ARM Controllers using C – Conditional Statements, Loop Statements, debugging, single stepping, breakpoints, pointers and data structures, variables, numbers and parameter passing. **(8 Hrs) [Blooms level selected: Application Level]**

REGISTRAR PRESIDENCY UNIVERSITY Registrar BANGALORE

Module 3: Memory Management and Device Driver Concepts: Introduction to Memory Organization, Memory Architectures, Memory Segments, Data Memory, Special Keywords (Const, Extern & Static), The Stack, The Heap, Code Memory, Practice on Memory Manipulation Software, Incorporate Memory Manipulation Software into the build system and Evaluation of some Test Functions. Linux - Scripting and Configuration, Kernel Building, Building Libraries and Utilities, Generic Device Driver Development Concepts, Linux Device Drivers. **(14 Hrs. Application Level) [Blooms level selected: Synthesis Level]**

DELIVERY PROCEDURE (PEDAGOGY):

Lectures will be conducted with the aid of online mode (MS Team), multi-media projector, blackboard and chalk.

- Assignments based on course contents will be given to the students at the end of each unit/topic and will be evaluated at regular intervals.
- Edhitch Quizzes will be conducted from time to time.
- Participative Learning: Seminar on important topics for development of quality and secure software for Embedded Systems will be arranged in a **flipped class – group and/or individual space** mode.
- Project Based Learning: Students will develop a working software for any typical embedded application as partial fulfillment of the course in the form of a Software Development Project, either in a group or as an individual.

REFERENCE MATERIALS: Textbooks, reference books, any other resources, like webpages.

Text Book(s):

1. Joseph Yiu, "*The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors*," 3rd Edition, Newnes.

Reference Book(s):

5. Michael Barr and Anthony Massa, "*Programming Embedded Systems with C and GNU Development Tools*," O'Reilly.
6. Haring D.D. et al., "Embedded Software Development With C," Springer.
7. Jane W S Liu, "Real – Time Systems", Prentice Hall, 2000.
8. Class Notes (CN).

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Video lectures on "Embedded System using Arm" by Prof. Dr.Indranil Sen Gupta, IIT KGP \

Lecture 01: Introduction to Embedded Systems - YouTube

2. Lecture series on Embedded Systems by Dr.Santanu Chaudhury,Dept. of Electrical Engineering, IIT

Delhi . For more details on NPTEL visit http://nptel.ac.in

E-content:

1.Camposano, R., & Wilberg, J. (1996). Embedded system design. Design Automation for Embedded

Systems, 1(1), 5-50. Embedded system design | SpringerLink

2. Ryu, S., & Kim, S. C. (2020). Embedded identification of surface based on multirate sensor fusion with deep neural network. IEEE embedded systems letters, 13(2), 49-52. Embedded Identification of Surface Based on Multirate Sensor Fusion With Deep Neural Network | IEEE Journals & Magazine | IEEE Xplore

Presidency University Library Link :- https://presiuniv.knimbus.com/user#/home

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

GUIDELINES TO STUDENTS:

Dear Students

Firstly I will ask you this – do NOT think of the course just as a course and count of credits to be met. This course deals with the software development practices which and Embedded Developer has to adopt. Therefore, start writing some basic level codes for accessing input and outputs ports and gradually move towards accessing on-chip as well as off-chip peripherals. I will be periodically sharing materials for various applications which you need to understand and develop your codes. **Initially, I will demonstrate working examples using simulators and on kits and later on you will do**. By the end of the semester you will all be able to implement your own mini projects on KEIL IDE for various embedded applications using ARM Cortex controller. **Together we will** create a healthy and fruitful learning environment.

COURSE SCHEDULE: (This is a macro level planning. Mention the unit wise expected starting and ending dates along with the tests/assignments/quiz and any other activities) [allot about 75% for delivery, about 10 to 12% for Evaluation Discussion, about 10 to 15% on integrating the learning Modules within the course and to the program]

Sl. No.	ACTIVITY	STARTING DATE	CONCLUDING DATE	TOTAL NO. OF PERIODS
1.	Over View of the course and program integration			1
2.	Module : 01			7
3.	Module: 02			8
4.	Project Proposal Discussion			1
5.	Mid Sem. Exam. Review			1
6.	Mid Sem. Exam. Discussion			1
7.	Integration of M1 and M2 to Course Project			1
8.	Module - 03			6
9.	Course Integration / Seminar			1
10.	Module - 03 (Continued)			8
11.	Course Project Progress Review			1
12.	Project Submission and Evaluation			3
13.	End Term Exam Review			1

SCHEDULE OF INSTRUCTION:

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

Sl. No	Session No / Date*	Lesson Title	Topics	CO No	Delivery Mode	Reference
1.	L1	Overview and integration	Program integration		Online Mode (MS Teams)	CN
2.	L2		Introduction to Embedded Systems Software Development	1		T1 - Ch 2, CN
3.	L3		Review of Embedded Systems and Application Areas	1		R1 - Ch 1, R2 - Ch 1, CN
4.	L4	Software Development Processes	Fundamentals of Software Engineering and Development Processes	1		T1 - Ch 2, R2 - Ch 2, CN
5.	L5		Embedded Software: Safety, Security and Quality	1		CN
6.	L6	Embedded Software Modeling Concepts	Introduction to Embedded Software Modeling, Context Diagrams, State Charts	1		R2 - Ch 2, CN
7.	L7		Finite State Machines (FSMs)	1		R2 - Ch 2, CN
8.	L8		Modeling Languages for Embedded Software	1		CN
Completion of Module 1						
		Self-Learning Topic				
9.	L9	Review of C Programming Concepts	Introduction to C-Programming for Embedded Systems	2		R2 - Ch 4, CN
10.	L10		C-Programming Review (Cont…)	2		R2 - Ch 4, CN
11.	L11		Programming ARM Controllers using C – Conditional Statements	2		R2 - Ch 4, CN
12.	L12	C Programming Constructs	Programming ARM Controllers using C – Loop Statements	2		R2 - Ch 4, CN
13.	L13		Programming ARM Controllers using C – debugging, single stepping, breakpoints	2		R2 - Ch 4, CN

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

14.	L14		Programming exercises on above topics.			R2 - Ch 4, CN
		Self-Learning Topic				
15.	L15	C Programming Constructs	Programming ARM Controllers using C – pointers and data structures	2		R2 - Ch 4, CN
16.	L16		Programming ARM Controllers using C – variables, numbers and parameter passing	2		R2 - Ch 4, CN
17.	L17		Project Discussion – 1			
18.	L18		Mid Sem Exam. Review			
19.	L19		Mid Sem Exam. Discussion			
20.	L20		Course Integration	4		CN
21.	L21		Introduction to Memory Organization	4		T1 – Ch 6, R1 – Ch 6, CN
22.	L22		Memory Architectures	4		T1 – Ch 6, R1 – Ch 6, CN
23.	L23		Memory Segments, Data Memory	4		T1 – Ch 6, R1 – Ch 6, CN
24.	L24		Special Keywords (Const, Extern & Static)	4		T1 – Ch 6, R1 – Ch 6, CN
25.	L25		The Stack	4		T1 – Ch 6, R1 – Ch 6, CN
26.	L26		The Heap	4		T1 – Ch 6, R1 – Ch 6, CN

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

27.	L27		Project Discussion – 2			
28.	L28	Memory Manipulation	Practice on Memory Manipulation Software	4		CN
29.	L29		Methodology, Synchronizing Software and Processor with I/O.	4		CN
30.	L30		Code Memory	4		T1 – Ch 6, R1 – Ch 6, CN
31.	L31		Seminar			
32.	L32		Code Memory	4		T1 – Ch 6, R1 – Ch 6, CN
		Self-Learning Topic				
33.	L33	Memory Manipulation	Practice on Memory Manipulation Software	4		CN
34.	L34		Methodology, Synchronizing Software and Processor with I/O.	4		CN
35.	L35	Device Driver Concepts	Linux: Scripting and Configuration	4		R1 – Ch 12, CN
36.	L36		Linux: Kernel Building	4		R1 – Ch 12, CN
37.	L37		Linux: Building Libraries and Utilities	4		R1 – Ch 12, CN
38.	L38		Generic Device Driver Development Concepts	4		CN
39.	L39		Linux: Device Drivers	4		R1 – Ch 12, CN
40.	L40		Linux: Device Drivers	4		R1 – Ch 12, CN

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

41.	L41		Linux: Device Drivers	4		R1 – Ch 12, CN
42.	L42		Review of previous classes and discussion on outcome of previous classes			CN
Completion of Module 3						
43.	L43	Evaluation	Peer Code Reviews			-
44.	L44		Project Submission and Evaluation (Seminar)			-
45.	L45		Software Project Submission and Evaluation			
46.	L46		Course Integration & End Term Exam Review			

* These dates are only indicative - applicable to one section handled by subject IC. Dates will vary from section to section.

Self-Learning:

S.No	Topics	References
1.	A Case Study of an Embedded System Software Stack Layers.	Internet / Teacher / Open Source and Published materials
2.	A Case Study on Embedded Software Quality Assurance and Testing.	Internet / Teacher / Open Source and Published materials
3.	A Case Study on Life Critical Software Systems.	Internet / Teacher / Open Source and Published materials
4.	A Case Study on Software Security, Threats and Vulnerabilities.	Internet / Teacher / Open Source and Published materials

Topics relevant to "SKILL DEVELOPMENT": Introduction to Embedded Systems, C-Programming for Embedded Systems. Memory management concepts for C programming for Skill Development through Participative Learning techniques. This is attained through assessment component mentioned in course handout. This is attained through the **Presentation** as mentioned in the assessment component.

ASSESSMENT SCHEDULE:

S. No.	Assessment Type	Contents	CO Number	Duration In Hours	Marks	Weightage	Venue, DATE &TIME

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

1.	Assignment	All	ALL	-NA-	20	10	Throughout semester
2.	Seminar	Embedded System Design | SpringerLink	All	10 - 15 minutes per student	20	10	After T1
3.	Assignment Review of digital / e-resources from Pres. Univ. link given in the References Section - (Mandatory to submit screenshot accessing digital resource. Otherwise it will not be evaluated)	https://ieeexplore.ieee.org/document/5090623 https://ieeexplore.ieee.org/document/5472888 https://ieeexplore.ieee.org/document/5568178 https://ieeexplore.ieee.org/document/5440056	CO1& CO2	-	10	10	Will be announced one week prior to submission
4.	Mid Sem. Exam	M1, M2 and Partial M3	CO1,2,3	90 Minutes	50	25	
5.	End Term	All	All	3 hours	100	50	

COURSE CLEARANCE CRITERIA:

- Minimum Attendance is 75%
- Minimum Internal Marks 40% of 50 = 20
- Minimum End Term Marks = 30% of 50 = 15
- However, aggregate of Internal and End Term should be 40 Marks.
- All as per academic regulations.

CONTACT TIMINGS IN THE CHAMBER FOR ANY DISCUSSIONS:

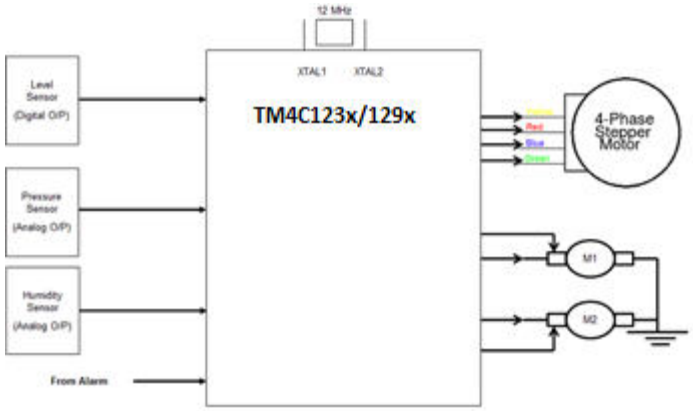
Every Tuesday 1pm

SAMPLE THOUGHT PROVOKING QUESTIONS:

SL NO	QUESTION	MARKS	CO. NO.	BLOOM'S LEVEL

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

1.	What do you understand by an embedded system software? Discuss at least four characteristics of an embedded system software.	6	CO1	L2
2.	Discuss the software development life cycle steps which are followed in waterfall method.	5	CO1	L2
3.	Discuss what qualities would you expect in an embedded software?	5	CO1	L2
4.	Recently there have been lot of controversies over use of Electronic Voting Machine (EVM) Systems in elections. You have been asked to design an "EVM System" to be used in elections. The system will have additional facility to webcast the voting process live to a central station using Wi-Fi/3G/4G connection by using a high resolution camera and/or tablet (as of now avoid VVPAT facility). Draw a FSM diagram considering various states, inputs and Outputs.	14	CO1	L3
5.	Draw the sequence diagram of a simple digital watch by indicating important steps.	10	CO1	L3
6.	Write a C program to generate a PWM waveform of 55% duty using the ARM controller TM4C123x / TM4C129x. Consider the default value for the clocks as supported by individual development boards.	14	CO3	L3
7.	Consider the figure shown below shows the layout of an Embedded System to be designed using the TM4C123x/129x microcontroller. Write a device driver for the individual modules shown such as for stepper motor control, dc motor control, timer and sensing inputs both digital as well as analog. 	30	CO4	L5

Target set for course Outcome attainment:

Sl. No	CO No.	Course Outcomes	Target set for attainment in percentage
1.	CO1	Summarize the concepts to develop software for real time embedded systems.	75%
2.	CO2	Develop efficient programs with IDE tools for embedded systems.	50%
3.	CO3	Categorize various open source compilers and tools for embedded software development.	35%

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

4.	CO4	Explain various concepts of memory management, device drivers, timers and interrupt systems, interfacing of devices, communications and networking in embedded systems.	35%

Signature of the course Instructor

This course has been duly verified Approved by the D.A.C.

Signature of the Chairperson D.A.C.

Course Completion Remarks &Self-Assessment. [This has to be filled after the completion of the course]

[Please mention about the course coverage details w.r.t. the schedule prepared and implemented. Any specific suggestions to incorporate in the course content. Any Innovative practices followed and its experience. Any specific suggestions from the students about the content, Delivery, Evaluation etc.]

Sl.no.	Activity As listed in the course Schedule	Scheduled Completion Date	Actual Completion Date	Remarks

Any specific suggestion/Observations on content/coverage/pedagogical methods used etc.:

Course Outcome Attainment:

Sl.no	C.O. No.	Course Outcomes	Target set for attainment in percentage	Actual C.O. Attainment In Percentage	Remarks on attainment &Measures to enhance the attainment
01	Co1				
02	Co2				

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

03	Co3				
04	Co4				

Name and signature of the Faculty member:

D.A.C. observation and approval:

BLOOM'S TAXONOMY

Learning Outcomes Verbs at Each Bloom Taxonomy Level to be used for writing the course Outcomes.

Cognitive Level	Illustrative Verbs	Definitions
Knowledge	arrange, define, describe, duplicate, identify, label, list, match, memorize, name, order, outline, recognize, relate, recall, repeat, reproduce, select, state	remembering previously learned information
Comprehension	classify, convert, defend, discuss, distinguish, estimate, explain, express, extend, generalize, give example(s), identify, indicate, infer, locate, paraphrase, predict, recognize, rewrite, report, restate, review, select, summarize, translate	grasping the meaning of information
Application	apply, change, choose, compute, demonstrate, discover, dramatize, employ, illustrate, interpret, manipulate, modify, operate, practice, predict, prepare, produce, relate schedule, show, sketch, solve, use write	applying knowledge to actual situations
Analysis	analyze, appraise, breakdown, calculate, categorize, classify, compare, contrast, criticize, derive, diagram, differentiate, discriminate, distinguish, examine, experiment, identify, illustrate, infer, interpret, model, outline, point out, question, relate, select, separate, subdivide, test	breaking down objects or ideas into simpler parts and seeing how the parts relate and are organized
Synthesis	arrange, assemble, categorize, collect, combine, comply, compose, construct, create, design, develop, devise, explain, formulate, generate, plan, prepare, propose, rearrange, reconstruct, relate, reorganize, revise, rewrite, set up, summarize, synthesize, tell, write	rearranging component ideas into a new whole

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

Evaluation	appraise, argue, assess, attach, choose, compare, conclude, contrast, defend, describe, discriminate, estimate, evaluate, explain, judge, justify, interpret, relate, predict, rate, select, summarize, support, value	making judgments based on internal evidence or external criteria

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

SCHOOL of ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Year: 2022-2023 (ODD) **Semester: I** **Section: SEC-01**

Course Title : Software for Embedded Systems

Course Code : ECE5008

Type of Skill : Employability Skill

Type of Activity : Participative Learning

Instructor in Charge : Dr. Noel Prashant Ratchagar.

Instructor for Section : Dr. Noel Prashant Ratchagar.

Date(s) of the activity : March 24, 2023 and March 28, 2023

Details about the activity : Students were asked to do a project based on real life applications. The students chose to do on digital camera and chocolate vending machine. A discussion for two days, pertaining to participative learning, was conducted with the assistance of an expert, Dr. Pramila.

Mode of Activity : Discussion on doing projects

Details of the students involved in the activity:

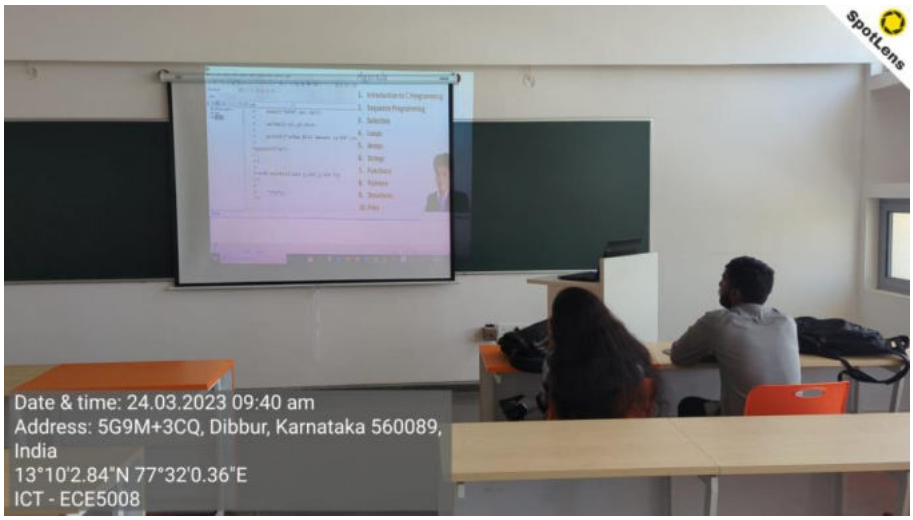
S.No	Name of the Student	Roll Number
1	CHORAGUDI DHANYA	20222ESV0001
2	SETTY REDDY VIKESH	20222ESV0002

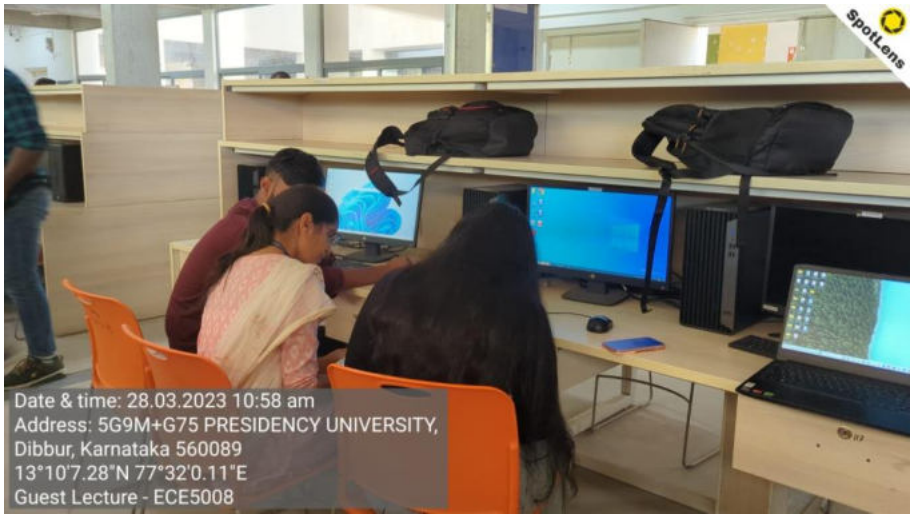
Remarks:

The activity focusses on developing their employability skills.

REGISTRAR

Sample Geo-tagged Photographs taken during the session:





Signature of Instructor:

Signature of Instructor In-Charge :

HOD - ECE

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

Course Code: ECE5023	**Course Title: : ASIC Design and Modelling** **Type of Course: Program Core Theory**		**L-P-C**	3	0	3
Version No.	1.0				
Course Pre-requisites	**Basic concepts of MOSFETs, Digital Design, Embedded Systems and Interfacing, Hardware Description Language**				
Anti-requisites	**NIL**				
Course Description	**This course aims to provide a strong foundation to understand the design of Application Specific Integrated Circuits (ASICs) design for real time digital systems. This course insight into the implementation Strategies for Digital ICs: Custom IC design, Cell-based design methodology. Array based implementation approaches critical physical design issues for future computing systems, and System-On-Chip (SOC) designs. Also, the course analyzes the timing issues in combinational and sequential logic design to represent the physical IC design procedures namely Partitioning, Floor Planning, Placement and Routing with its types.**				
Course Objective	**The objective of the course is to familiarize the learners with the concepts of ASIC Design and Modelling and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.**				
Course Outcomes	**On successful completion of this course the students shall be able to:** 1. Demonstrate the characteristic of ASICs with Programming technologies of Logic Devices 2. Summarize the physical design process utilized in the design of ASICs 3. Analyze the faults and timing issues in the developed ASIC design 4. Classify the FPGA devices based on the architecture and design technology				
Course Content:					
Module 1	**Overview of ASIC and PLD**	Quiz	Memory Recall-based Quizzes		**10 sessions**
Topics: Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs					
Module 2	**ASIC Physical Design**	Assignment / Quiz	Memory Recall-based Quizzes		**10 sessions**

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

Topics:

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction – DRC.

Module 3	**Logic Synthesis, Simulation and Testing**	Assignment	Analysis and Verification	**10 sessions**

Topics:

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

Module 4	**FPGA Testing**	Assignment	Memory Recall-based Quizzes	**10 sessions**

Topics:

Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology - mapping for FPGAs ,FPGA Verification Techniques, PLB Architecture, BIST Architecture using Diagnostic Procedure Xilinx XC4000 - ALTERA's FLEX 8000/10000, and their speed performance

Project Work/Assignment:

1. Case Studies: At the end of the course students will be given case studies on Xilinx XC4000 and ALTERA's FLEX 8000 in the appropriate format.

2. Book/Article review: At the end of each module a book reference or an article topic will be given to an individual or a group of students. They need to refer to the library resources and write a report on their understanding of the assigned article in the appropriate format. **Presidency University Library Link .**

3. Presentation: There will be a seminar presentation, where the students will be given a topic. They will have to explain/teach the working and discuss the applications for the same.

4. Project Assignment: (Don't be specific)

Reconfigured VLSI architecture for DSRC applications. This topic mainly gives information on how ITS concepts can be used to provide more safety and leisure in traveling at a low cost.

DSRC (Dedicated short-range communication) is wireless communication technology. It enables different users to be better informed, and make safer, more coordinated, and advanced use of transportation networks. ITS has provided this unique service. DSRC can be classified into two categories. These are automobile to automobile and automobile to roadside.

DSRC uses FM0 and Manchester codes for encoding. The diversity between the 2 codes limits the potential to design fully reused VLSI architecture for both codes. SOLS is used to design fully reused VLSI architecture.

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

In this VLSI design project, with this the Similarity oriented logic simplification techniques (SOLS) technique and many more techniques discussed above result in improvement in HUR, area optimization, reduced power consumption, lower latency, and elimination of many other limitations on hardware utilization.

The FM0 and Manchester encoders are designed with these techniques to achieve high speed and fully reconfigured VLSI architecture for the application system.

Assignment 1: Implement Programmable Logic Devices: ROMs and EPROMs – PLA –PAL using Cadence tool

Assignment 2: Case studies

1. M.J.S .Smith, "*Application Specific Integrated Circuits*", 1st Edition, Addison – Wesley Longman Inc., 1997.
2. Naveed Sherwani, "*Algorithms for VLSI Physical design automation*", 3rd Edition, Springer International edition, 2005.

Reference(s):

Reference Book(s):

1. Himanshu Bhatnagar, "*Advanced ASIC Chip Synthesis*",2nd Edition, Kluwer Academic Publisher, 2002
2. Farzad Nekoogar, "*Timing Verification of Application-Specific Integrated Circuits*", 1st Edition, Farzad Nekoogar, Prentice-Hall. 1999.
3. J. Bhaskar, "Verilog HDL for synthesis",1st Edition, BS Publication,2004:

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL Course on VLSI Design Verification and test, by Dr. Santosh Biswas, Prof.Jatindra Kumar Deka, Prof.Arnab sarkar, IIT Guwahati. https://nptel.ac.in/courses/117103125
2. NPTEL Course on VLSI Circuits, by Prof. S. Srinivasan, IIT Madras. https://nptel.ac.in/courses/117106092

E-content:

1. C.-Y. Lee; F.V.M. Catthoor; H.J. de Man, "An efficient ASIC architecture for real-time edge detection", IEEE Transactions on Circuits and Systems, Volume: 36, Issue: 10, October 1989, pp: 1350-1359. https://ieeexplore.ieee.org/document/44350
2. Masudul Hassan Quraishi , Erfan Bank Tavakoli, and Fengbo Ren, "A Survey of System Architectures and Techniques for FPGA Virtualization", IEEE Transactions on Parallel and Distributed Systems, Vol. 32, No. 9, September 20, pp: 2216-2230. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9369140
3. MJ, S. P. Comprehensive Study of Popular VLSI Test Scan Architecture. https://www.ijert.org/comprehensive-study-of-popular-vlsi-test-scan-architecture

Topics relevant to "EMPLOYABILITY SKILLS": ASIC Design and Floor planning," FPGA architecture and FPGA fabrics, FPGA testing for developing Employability Skills through

Participative Learning techniques. This is attained through assessment component mentioned in course handout.	
Catalogue prepared by	Mrs. Aruna Dore
Recommended by the Board of Studies on	15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Meeting No. 18th , Dated 03/08/2022

PRESIDENCY UNIVERSITY

(Established under the Presidency University Act, 2013 of the Karnataka Act 41 of 2013)

A-2 [2022] COURSE HAND OUT [Integrated Course]

SCHOOL: Engineering **DEPT.:** Electronics and Communication Engineering **DATE OF ISSUE: 27/08/2022**

NAME OFTHE PROGRAM : M.Tech

P.R.C. APPROVALREF : PU/AC-18.4/ECE15/ESV/2022-24

SEMESTER/YEAR : 1st Sem/1st Year

COURSE TITLE&CODE : ASIC Design and Modelling & ECE5009

COURSE CREDITSTRUCTURE: **3 Credits (L=3,T=0, P=0, C=3)**

CONTACT HOURS : 3 Hours/Week

COURSE INSTRUCTOR : **Dr. Joseph Anthony Pratap**

PROGRAM OUTCOMES:

Graduates of the M. Tech. Program in Embedded System and VLSI Design will be able to:

PO1. An ability to apply knowledge of mathematics, science and engineering in practice.

REGISTRAR

PO2. **An ability to identify, critically analyze, formulate and solve engineering problems with comprehensive knowledge in the area of specialization.**.

PO3. An ability to select modern engineering tools and techniques and use them with dexterity.

PO4. An ability to design a system and process to meet desired needs within realistic constraints such as health, safety, security and manufacturability.

PO5. An ability to contribute by research and innovation to solve engineering problems.

PO6. An ability to devise and conduct experiments, interpret data and provide well informed conclusions.

PO7. An ability to understand the impact of engineering solutions in a contemporary, global, economic, environmental, and societal context for sustainable development.

PO8. An ability to function professionally with ethical responsibility as an individual as well as in multidisciplinary teams with positive attitude.

PO9. An ability to communicate effectively.

PO10. **An ability to appreciate the importance of goal setting and to recognize the need for life-long reflective learning.**

COURSE PREREQUISITES:

Before attempting this course the student should have prior knowledge Basic concepts of MOSFETs, Digital Design, Embedded Systems and Interfacing, Hardware Description Language

COURSE DESCRIPTION:

This course aims to provide a strong foundation to understand the design of Application Specific Integrated Circuits (ASICs) design for real time digital systems. This course insight into the implementation Strategies for Digital ICs: Custom IC design, Cell-based design methodology. Array based implementation approaches critical physical design issues for future computing systems, and System-On-Chip (SOC) designs. Also, the course

analyzes the timing issues in combinational and sequential logic design to represent the physical IC design procedures namely Partitioning, Floor Planning, Placement and Routing with its types.

Course Objective:

The objective of the course is to familiarize the learners with the concepts of ASIC Design and Modelling and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.

COURSE OUTCOMES: On successful completion of the course the students shall be able to:

1. Demonstrate the characteristic of ASICs with Programming technologies of Logic Devices
2. Summarize the physical design process utilized in the design of ASICs
3. Analyze the faults and timing issues in the developed ASIC design
4. Classify the FPGA devices based on the architecture and design technology

MAPPING OF C.O. WITH P.O

CO N0.	PO 1	PO 2	PO 3	PO 5	PO 6	PO 8	PO 10
1	H	M	H	M	M	L	L
2	H	H	M	H	L	L	L
3	H	M	H	M	H	L	L
4	H	L	M	M	H	L	L

COURSE CONTENT (SYLLABUS):

Module 1: Overview of ASIC and PLD [9 Hours] [Comprehension]

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

Module 2: ASIC Physical Design [8 Hours] [Application]

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction – DRC.

Module 3: Logic Synthesis, Simulation and Testing [9 Hours] [Analyze]

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools - EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

Module 4: FPGA Testing **[9 Hours] [Application]**

Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology - mapping for FPGAs, Xilinx XC4000 - ALTERA's FLEX 8000/10000, and their speed performance Case studies: Altera MAX 5000 and 7000 - Altera MAX 9000 – Spartan II and Virtex II FPGAs - Apex and Cyclone FPGAs

SKILL SETS TO BE DEVLOPED:

1. An attitude of enquiry.
2. Confidence and ability to tackle new problems.
3. Ability to interpret events and results.
4. Ability to work as a leader and as a member of a team.
5. Assess errors in systems/processes/programs/computations and eliminate them.
6. Observe and measure physical phenomena.
7. Write reports.
8. Select suitable equipment, instrument, materials & software
9. Locate faults in system/Processes/software.
10. Manipulative skills for setting and handling systems/Process/Issues
11. The ability to follow standard /Legal procedures.
12. An awareness of the Professional Ethics.
13. Need to observe safety/General precautions.
14. To judge magnitudes/Results/issues without actual measurement/actual contacts

DELIVERY PROCEDURE (PEDAGOGY):

Lectures will be conducted with the aid of multi-media projector, blackboard, etc. Assignments based on course contents will be given to the students at the end of each unit/topic and will be evaluated at regular intervals.
Self-Learning Topics: Programmable Logic Devices: ROMs and EPROMs – PLA –PAL.

Participative Learning: Altera MAX 5000 and 7000 - Altera MAX 9000
Learning: Optimizing the ASIC design parameters from Presidency University E-resources

REFERENCE MATERIALS:

(i) Text Book(S)

1. M.J.S .Smith, "*Application Specific Integrated Circuits*", 1st Edition, Addison – Wesley Longman Inc., 1997.
2. Naveed Sherwani, "*Algorithms for VLSI Physical design automation*", 3rd Edition, Springer International edition, 2005.

(ii) Reference Book(S)

1. J. Bhaskar, "*Verilog HDL for synthesis*", 1st Edition, BS Publication, 2004.
2. Himanshu Bhatnagar, "*Advanced ASIC Chip Synthesis*",2nd Edition, Kluwer Academic Publisher, 2002.
3. Farzad Nekoogar, "*Timing Verification of Application-Specific Integrated Circuits*", 1st Edition, Farzad Nekoogar, Prentice-Hall. 1999.
4. Sachin Sapatnekar, "*Timing*", 1st Edition, Kluwer Academic Publishers, 2004, New York.

(iii) Class Notes

1. NPTEL Course on VLSI Design Verification and test, by Dr. Santosh Biswas, Prof.Jatindra Kumar Deka, Prof.Arnab sarkar, IIT Guwahati. https://nptel.ac.in/courses/117103125
2. NPTEL Course on VLSI Circuits, by Prof. S. Srinivasan, IIT Madras. https://nptel.ac.in/courses/117106092
3. PG Level Advanced Certification Programme in "VLSI Chip Design" https://iisc.talentsprint.com/vlsi/index.html

(iv) E-content

4. C.-Y. Lee; F.V.M. Catthoor; H.J. de Man, "An efficient ASIC architecture for real-time edge detection", IEEE Transactions on Circuits and Systems, Volume: 36, Issue: 10, October 1989, pp: 1350-1359. https://ieeexplore.ieee.org/document/44350
5. Masudul Hassan Quraishi , Erfan Bank Tavakoli, and Fengbo Ren, "A Survey of System Architectures and Techniques for FPGA Virtualization", IEEE Transactions on Parallel and Distributed Systems, Vol. 32, No. 9, September 20, pp: 2216-2230. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9369140
6. Rohit B. Chaurasiya, and Rahul Shrestha, "Design and ASIC-Implementation of Hardware-Efficient Cooperative Spectrum-Sensor for Data Fusion Based Cognitive Radio Network", IEEE Transactions on Consumer Electronics (Early Access), 2022. https://ieeexplore.ieee.org/document/9757138
7. Matías J. Garrido, Fernando Pescador, M. Chavarrías, P. J. Lobo, and César Sanz, "A High Performance FPGA-Based Architecture for the Future Video Coding Adaptive Multiple Core Transform", IEEE Transactions on Consumer Electronics, Vol. 64, No. 1, February 2018, pp: 53-80. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8307423

(v) GUIDELINES TO STUDENTS:

1. Students are required to maintain classwork which will be evaluate at the end of every month
2. Students are required to strictly adhere to assignment deadlines.
3. Students are required to actively participate in classroom discussions and other activities which is planned in the classroom.

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

4. Students are required to have minimum of 75% of attendance to be eligible to attend exam.

(vi) Presidency University Library Link :- https://presiuniv.knimbus.com/user#/home

COURSE SCHEDULE:

Sl. No.	ACTIVITY	STARTING DATE	CONCLUDING DATE	TOTAL NUMBER OF PERIODS
1.	Over View of the course			
2.	Module : 01			
3.	Module: 02			
4.	Project Proposal Discussion			
5.	Mid Sem. Exam			
6.	Module - 03			
7.	Module - 04			
8.	Quiz			
9.	Assignment			
10.	Integration of M1 and M2 to Course Project			
11.	Instruction last day			

SCHEDULE OF INSTRUCTION:

Sl. No	Session/ Date	Lesson Title	Topics	CO	Delivery Mode	Reference
1.	L1	Course Description	Over View of the course	1	Lecture	CN
Module-1						
2.	L2	Overview of ASIC and PLD	Types of ASICs	1	Lecture	T1, CN
3.	L3	Overview of ASIC and PLD	Design flow	1	Lecture	T1, CN
4.	L4	Overview of ASIC and PLD	CAD tools used in ASIC Design	1	Lecture	T1, CN

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

5.	L5	Overview of ASIC and PLD	Programming Technologies: Anti-fuse	1	Lecture	T1, CN
6.	L6	Overview of ASIC and PLD	Static RAM	1	Lecture	T1, CN
7.	L7	Overview of ASIC and PLD	EPROM and EEPROM technology	1	Lecture	T1, CN
8.	L8	Overview of ASIC and PLD	Programmable Logic Devices: ROMs and EPROMs	1	Lecture	T1, CN
9.	L9	Overview of ASIC and PLD	PLA –PAL	1	Lecture	T1, CN
10.	L10	Overview of ASIC and PLD	Gate Arrays, CPLDs and FPGAs	1	Lecture	T1, CN
Module – 2						
11.	L11	ASIC Physical Design	System partition	2	Lecture	T1, CN
12.	L12	ASIC Physical Design	Partitioning, partitioning methods	2	Lecture	T1, CN
13.	L13	ASIC Physical Design	Interconnect delay models and measurement of delay	2	Lecture	T1, CN
14.	L14	ASIC Physical Design	Floor planning	2	Lecture	T2, CN
15.	L15	ASIC Physical Design	Placement	2	Lecture	T2, CN
16.	L16	ASIC Physical Design	Routing: global routing	2	Lecture	T2, CN
17.	L17	ASIC Physical Design	Detailed routing,	2	Lecture	T2, CN

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

			Special routing			
18.	L18	ASIC Physical Design	Circuit extraction, DRC	2	Lecture	T2, CN
19.	L19	ASIC Physical Design	Project Proposal Discussion	2	Lecture	T2, CN
20.	L20	Overview of ASIC and PLD & ASIC Physical Design	Mid Sem. Exam. Review	2	Lecture	T1, T2, CN
21.	L21		Integration of M1 and M2 to Course Project	2	Lecture	T1, T2, CN
Module-3						
22.	L22	Logic Synthesis, Simulation and Testing	Design systems, Logic Synthesis	3	Lecture	T1, CN
23.	L23	Logic Synthesis, Simulation and Testing	Half gate ASIC, Schematic entry	3	Lecture	T1, CN
24.	L24	Logic Synthesis, Simulation and Testing	Low level design language, PLA tools	3	Lecture	R1,CN
25.	L25	Logic Synthesis, Simulation and Testing	EDIF, CFI design representation.	3	Lecture	R1,CN
26.	L26	Logic Synthesis, Simulation and Testing	Verilog and logic synthesis	3	Lecture	R1,CN
27.	L27	Logic Synthesis, Simulation and Testing	VHDL and logic synthesis	3	Lecture	R1, CN
28.	L28	Logic Synthesis, Simulation and Testing	Types of simulation	3	Lecture	R1,CN

REGISTRAR
PRESIDENCY UNIVERSITY Registrar BANGALORE

29.	L29	Logic Synthesis, Simulation and Testing	Boundary scan test, fault simulation	3	Lecture	R2, CN
30.	L30	Logic Synthesis, Simulation and Testing	Automatic test pattern generation	3	Lecture	R2, CN
Module-4						
31.	L31	FPGA Testing	Field Programmable gate arrays Logic blocks, Routing architecture,	4	Lecture	T1, CN
32.	L32	FPGA Testing	Design flow technology, mapping for FPGAs,	4	Lecture	T1, CN
33.	L33	FPGA Testing	Xilinx XC4000, and their speed performance	4	Lecture	T1, R3, CN
34.	L34	FPGA Testing	ALTERA's FLEX 8000/10000, and their speed performance	4	Lecture	T1, R3, CN
35.	L35	FPGA Testing	Case studies: Altera MAX 5000 and 7000	4	Lecture	T1, CN
36.	L36	FPGA Testing	Altera MAX 9000	4	Lecture	T1, R4, CN
37.	L37	FPGA Testing	Spartan II FPGAs	4	Lecture	T1, R4, CN
38.	L38	FPGA Testing	Virtex II FPGAs	4	Lecture	T1, CN

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

39.	L39	FPGA Testing	Apex and Cyclone FPGAs	4	Lecture	T1, CN
40.	L40	Project Alternate Assesment	Course Project Progress Review	4	Project Work	--
41.	L41	Project Alternate Assesment	Project Submission and Evaluation	4	Project Work	--
42.	L42		End Term Exam Review	4	Lecture	T1, T2, CN

Topics relevant to "EMPLOYABILITY SKILLS": ASIC Design and Floor planning," FPGA architecture and FPGA fabrics, FPGA testing for developing Employability Skills through Participative Learning techniques. This is attained through the Presentation as mentioned in the assessment component.

ASSESSMENT SCHEDULE FOR THEORY COMPONENT:

Sl.no	Assessment type	Contents	Course outcome Number	Duration In Hours	Marks	Weightage	Venue, DATE &TIME
1	Presentation	Module 1 to 4	1,2,3,4		10	15	
2	Quiz 1	Module 1, Module 2	1,2	15 mins	10	05	
3	Mid Exam	Modules 1,2	1,2,3,4	1 Hour & 30 mins	50	25	Offline Exam
4	Assignment Review of digital / e-resources from Pres. Univ. link given in the References Section - (Mandatory to submit screenshot accessing digital resource. Otherwise it will not be evaluated)	https://ieeexplore.ieee.org/document/5090623 https://ieeexplore.ieee.org/document/5472888 https://ieeexplore.ieee.org/document/5568178 https://ieeexplore.ieee.org/document/54400	CO1& CO2	-	10	10	Will be announced one week prior to submission

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

		56					
5	End Term Exam	Modules 1 to 4	1,2,3,4	3 Hours	100	50	Offline Exam

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

COURSE CLEARANCE&EVALUATION CRITERIA:

A minimum of 75% attendance is required for both lab and theory separately to attend the end term exam. Make-up policy will be only as per academic regulation.

Method of Assessment for Courses with Credit Structure (L –T -0) or (L – 0 – 0)			
	Components of Continuous Assessments	**Weightage (% of Total Marks)**	**Duration of Assessment**
1.	Mid Term	25%	1.5 hour
2.	This Component of continuous assessment shall consist of at least TWO (02) of thefollowing: (1) Assignment(s) (2) Quiz (3) Technical Seminar / Report (4) Attendance / Class participation (5) Assessment on self-learning topic(s), or (6) Any other type of assessment as prescribed in the concerned Course Handout.	25%	NA
3.	End Term Final Examinations	50%	3 hours
	Total	**100%**	

MAKEUP POLICY:

If the student misses an evaluation component, he/she may be granted a make-up. In case of an absence that is foreseen, make-up request should be personally made to the Instructor-in-Charge, well ahead of the scheduled evaluation component. Reasons for unanticipated absence that qualify a student to apply for make-up include medical emergencies or personal exigencies. In such an event, the student should contact the Instructor-in-Charge as soon as practically possible.

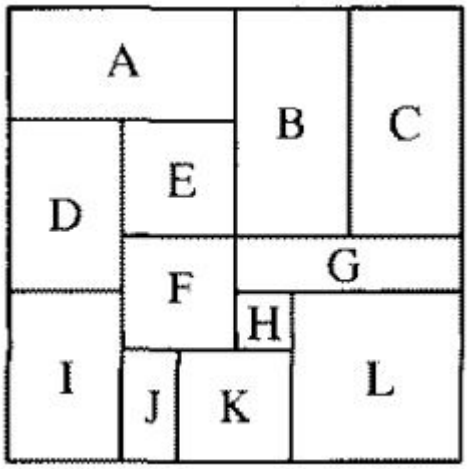
CONTACT TIMINGS IN THE CHAMBER FOR ANY DISCUSSIONS:

It will be announced in the class. Interested students may meet the Instructor In-charge during the Chamber Consultation Hour to clear doubts.

SAMPLE THOUGHT PROVOKING QUESTIONS:

SL NO	QUESTION	MARKS	COURSE OUTCOME NO	BLOOM'S LEVEL
1.	PLD are combination of AND & OR plane and is advanced has led to CPLD and FPGA. These digital controllers can be used in reality based on the requirement of the application. Distinguish between the different types of ASIC Circuits used in Real Time Applications	10	CO2	Analyze

REGISTRAR

2.	Floorplan determines the size, shape, and locations of modules in a chip and as such it estimates the total chip area, the interconnects, and, delay. Develop the Slicing Tree for the Floor plan shown in Fig.1.  Fig.1	10	CO3	Application
3.	The design of Processor requires complex arithmetic and logic unit to accomplish demands of Power, performance and Compatibility of application. Develop the RISC Processor design using the HDL Code.	10	CO1	Application
4	The Xilinx and Altera Devices are utilized in the design of complex addition circuit. Analyze the performance characteristic of tree based addition circuit of 12 bit resolution for the implementation in Xilinx and Altera device.	10	CO4	Analyze

Target set for course Outcome attainment:

Sl.no	C.O. No.	Course Outcomes	Target set for attainment in percentage
01	CO1	Demonstrate the characteristic of ASICs with Programming technologies of Logic Devices	60%
02	CO2	Summarize the physical design process utilized in the design of ASICs	60%
03	CO3	Analyze the faults and timing issues in the developed ASIC design	60%
04	CO4	Classify the FPGA devices based on the architecture and design technology	60%

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

Signature of the course Instructor Dr. JOSEPH ANTHONY PRATHAP

This course has been duly verified Approved by the D.A.C.

Signature of the Chairperson D.A.C.

Course Completion Remarks &Self-Assessment.[This has to be filled after the completion of the course]

[Please mention about the course coverage details w.r.t. the schedule prepared and implemented. Any specific suggestions to incorporate in the course content. Any Innovative practices followed and its experience. Any specific suggestions from the students about the content, Delivery, Evaluation etc.]

Sl.no.	Activity As listed in the course Schedule	Scheduled Completion Date	Actual Completion Date	Remarks
1	Over View of the course			
2	Module : 01			
3	Module: 02			
4	Assignment			
5	Test-1			
6	Module:03			
7	Module:04			
8	Assignment			
9	Test-2			

Any specific suggestion/Observations on content/coverage/pedagogical methods used etc.:

Course Outcome Attainment:

Sl.no	C.O. No.	Course Outcomes	Target set for attainment in percentage	Actual C.O. Attainment In Percentage	Remarks on attainment &Measures to enhance the attainment
01	CO1	Demonstrate the characteristic of ASICs with	60%		

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

		Programming technologies of Logic Devices			
02	CO2	Summarize the physical design process utilized in the design of ASICs	60%		
03	CO3	Analyze the faults and timing issues in the developed ASIC design	60%		
04	CO4	Classify the FPGA devices based on the architecture and design technology	60%		

Program Outcome Attainment:

PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10

Name and signature of the Course Instructor:

D.A.C. observation and approval:

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

BLOOM'S TAXONOMY

Learning Outcomes Verbs at Each Bloom Taxonomy Level to be used for writing the course Outcomes.

Cognitive Level	Illustrative Verbs	Definitions
Knowledge	arrange, define, describe, duplicate, identify, label, list, match, memorize, name, order, outline, recognize, relate, recall, repeat, reproduce, select, state	remembering previously learned information
Comprehension	classify, convert, defend, discuss, distinguish, estimate, explain, express, extend, generalize, give example(s), identify, indicate, infer, locate, paraphrase, predict, recognize, rewrite, report, restate, review, select, summarize, translate	grasping the meaning of information
Application	apply, change, choose, compute, demonstrate, discover, dramatize, employ, illustrate, interpret, manipulate, modify, operate, practice, predict, prepare, produce, relate schedule, show, sketch, solve, use write	applying knowledge to actual situations
Analysis	analyze, appraise, breakdown, calculate, categorize, classify, compare, contrast, criticize, derive, diagram, differentiate, discriminate, distinguish, examine, experiment, identify, illustrate, infer, interpret, model, outline, point out, question, relate, select, separate, subdivide, test	breaking down objects or ideas into simpler parts and seeing how the parts relate and are organized
Synthesis	arrange, assemble, categorize, collect, combine, comply, compose, construct, create, design, develop, devise, explain, formulate, generate, plan, prepare, propose, rearrange, reconstruct, relate, reorganize, revise, rewrite, set up, summarize, synthesize, tell, write	rearranging component ideas into a new whole
Evaluation	appraise, argue, assess, attach, choose, compare, conclude, contrast, defend, describe, discriminate, estimate, evaluate, explain, judge, justify, interpret, relate, predict, rate, select, summarize, support, value	making judgments based on internal evidence or external criteria

REGISTRAR

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

SCHOOL of ENGINEERING
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Year: 2022-2023 (ODD) **Semester: M.Tech.** **Section: ESV**

Course Title : ASIC Design.

Course Code : ECE5009

Type of Skill : Skill Development

Type of Activity : Participative Learning

Instructor in Charge : Dr. JOSEPH ANTHONY PRATHAP.

Instructor for Section : Dr. JOSEPH ANTHONY PRATHAP

Details about the activity : Students were asked to present on any Topic in ASIC Design

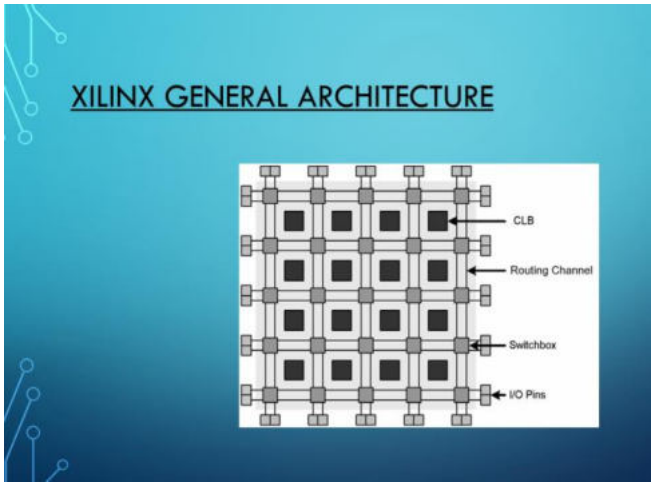
Mode of Activity : Presentation on Xilinx and Altera Configuration Blocks

Details of the students involved in the activity:

S.No	Name of the Student	Roll Number
1	CHARAGUDI DHANYA	20222ESV0001
2	SETTY REDDY VIGNESH	20222ESV0002

Date of presentation: 20.4.23

A.



REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE

Remarks:

- By **participating in this presentation**, students **learned** about the block diagram of Xilinx and Altera devices.
- This learning will **Develop their Skills** in analyzing the performance of FPGA in real time

Signature of Instructor: ZARA

Signature of Instructor In-Charge : ZARA

HOD - ECE

REGISTRAR

PRESIDENCY UNIVERSITY Registrar BANGALORE