PRESIDENCY UNIVERSITY
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PROGRAMME REGULATIONS & CURRICULUM

2024-26

PRESIDENCY SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MASTER OF TECHNOLOGY
EMBEDDED SYSTEM & VLSI

PRESIDENCY UNIVERSITY

Presidency University Act, 2013 of the Karnataka Act No. 41 of 2013 | Established under Section 2(f) of UGC Act, 1956
Approved by AICTE, New Delhi

PRESIDENCY SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Program Regulations and Curriculum

2024-2026

MASTER OF TECHNOLOGY (M.Tech.) in

Embedded System & VLSI

based on Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

(As amended up to the 24th Meeting of the Academic Council held on 3rd August 2024. This document supersedes all previous guidelines)

Regulations No: PU/AC-24.10/ECE19/ESV/2024-26

Resolution No. 10 of the 24th Meeting of the Academic Council held on 16th July, 2024, and ratified by the Board of Management in its 23rd Meeting held on 19th July, 2024.

AUGUST-2024

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PART A – PROGRAM REGULATIONS

1. Vision & Mission of the University and the School / Department

1.1 Vision of the University

To be a Value-driven Global University, excelling beyond peers and creating professionals of integrity and character, having concern and care for society.

1.2 Mission of the University

- Commit to be an innovative and inclusive institution by seeking excellence in teaching, research and knowledge-transfer.
- Pursue Research and Development and its dissemination to the community, at large.
- Create, sustain and apply learning in an interdisciplinary environment with consideration for ethical, ecological and economic aspects of nation building.
- Provide knowledge-based technological support and services to the industry in its growth and development.
- To impart globally-applicable skill-sets to students through flexible course offerings and support industry's requirement and inculcate a spirit of new-venture creation.

1.3 Vision of Presidency School of Engineering

To be a value based, practice-driven School of Engineering and Technology, committed to developing globally-competent Engineers, dedicated to transforming Society.

1.4 Mission of Presidency School of Engineering

- Cultivate a practice-driven environment with a contemporary Learning-pedagogy, integrating theory and practice.
- Attract and nurture world-class faculty to excel in Teaching and Research, in the field of Core Engineering.
- Establish state-of-the-art facilities for effective Teaching and Learning-experiences.
- Promote Interdisciplinary Studies to nurture talent and impart relevant skill-sets for global impact.
- Instil Entrepreneurial and Leadership Skills to address Social, Environmental, and Community-needs.

1.5 Vision of Department of Electronics and Communication Engineering

To be a value-based, industry driven Electronics and Communication Engineering Department committed to develop globally competent Electronics and Communication Engineering professionals dedicated to transform the society.

1.6 Mission of Department of Electronics and Communication Engineering

- Committed to inculcate application of Engineering knowledge, develop problem analysis and solving skills to be able to investigate complex engineering problems with modern tools.
- Create value-driven engineering professionals who are sensitive to societal concerns of environmental sustainability through ethical conduct.
- Develop excellent communication abilities with core skills of project management and team work.
- Imbibe passion for lifelong learning with individual growth path.
- Commitment towards excellence in Electronics and Communication Engineering education through advancements in research and innovation.

- Design flexible course contents in disciplinary, interdisciplinary and research areas to enhance student's competitiveness.

2. Preamble to the Program Regulations and Curriculum

This is the subset of Academic Regulations and it is to be followed as a requirement for the award of M.Tech degree.

The Curriculum is designed to take into the factors listed in the Choice Based Credit System (CBCS) with focus on Social Project Based Learning, Industrial Training, and Internship to enable the students to become eligible and fully equipped for employment in industries, choose higher studies or entrepreneurship.

In exercise of the powers conferred by and in discharge of duties assigned under the relevant provision(s) of the Act, Statutes and Academic Regulations of the University, the Academic Council hereby makes the following Regulations.

3. Short Title and Applicability

a. These Regulations shall be called the Master of Technology Degree Program Regulations and Curriculum 2024-2026.
b. These Regulations are subject to, and pursuant to the Academic Regulations.
c. These Regulations shall be applicable to the ongoing Master of Technology Degree Programs of the 2024-2026 batch, and to all other Master of Technology Degree Programs which may be introduced in future.
d. These Regulations shall supersede all the earlier Master of Technology Degree Program Regulations and Curriculum, along with all the amendments thereto.
e. These Regulations shall come into force from the Academic Year 2024-2025.

4. Definitions

In these Regulations, unless the context otherwise requires:

a. *"Academic Calendar" means the schedule of academic and miscellaneous events as approved by the Vice Chancellor;*
b. *"Academic Council" means the Academic Council of the University;*
c. *"Academic Regulations" means the Academic Regulations, of the University;*
d. *"Academic Term" means a Semester or Summer Term;*
e. *"Act" means the Presidency University Act, 2013;*
f. *"AICTE" means All India Council for Technical Education;*
g. *"Basket" means a group of courses bundled together based on the nature/type of the course;*
h. *"BOE" means the Board of Examinations of the University;*
i. *"BOG" means the Board of Governors of the University;*
j. *"BOM" means the Board of Management of the University;*
k. *"BOS" means the Board of Studies of a particular Department/Program of Study of the University;*
l. *"CGPA" means Cumulative Grade Point Average as defined in the Academic Regulations;*
m. *"Clause" means the duly numbered Clause, with Sub-Clauses included, if any, of these Regulations;*
n. *"COE" means the Controller of Examinations of the University;*
o. *"Course In Charge" means the teacher/faculty member responsible for developing and*

organising the delivery of the Course;

p. *"Course Instructor" means the teacher/faculty member responsible for teaching and evaluation of a Course;*

q. *"Course" means a specific subject usually identified by its Course-code and Course-title, with specified credits and syllabus/course-description, a set of references, taught by some teacher(s)/course-instructor(s) to a specific class (group of students) during a specific Academic Term;*

r. *"Curriculum Structure" means the Curriculum governing a specific Degree Program offered by the University, and, includes the set of Baskets of Courses along with minimum credit requirements to be earned under each basket for a degree/degree with specialization/minor/honours in addition to the relevant details of the Courses and Course catalogues (which describes the Course content and other important information about the Course). Any specific requirements for a particular program may be brought into the Curriculum structure of the specific program and relevant approvals should be taken from the BOS and Academic Council at that time.*

s. *"DAC" means the Departmental Academic Committee of a concerned Department/Program of Study of the University;*

t. *"Dean" means the Dean / Director of the concerned School;*

u. *"Degree Program" includes all Degree Programs;*

v. *"Department" means the Department offering the degree Program(s) / Course(s) / School offering the concerned Degree Programs / other Administrative Offices;*

w. *"Discipline" means specialization or branch of B.Tech. Degree Program;*

x. *"HOD" means the Head of the concerned Department;*

y. *"L-T-P-C" means Lecture-Tutorial-Practical-Credit – refers to the teaching – learning periods and the credit associated;*

z. *"MOOC" means Massive Open Online Courses;*

aa. *"MOU" means the Memorandum of Understanding;*

bb. *"NPTEL" means National Program on Technology Enhanced Learning;*

cc. *"Parent Department" means the department that offers the Degree Program that a student undergoes;*

dd. *"Program Head" means the administrative head of a particular Degree Program/s;*

ee. *"Program Regulations" means the Master of Technology Degree Program Regulations and Curriculum, 2024-2026;*

ff. *"Program" means the Master of Technology (M.Tech.) Degree Program;*

gg. *"PSOE" means the Presidency School of Engineering;*

hh. *"Registrar" means the Registrar of the University;*

ii. *"School" means a constituent institution of the University established for monitoring, supervising and guiding, teaching, training and research activities in broadly related fields of studies;*

jj. *"Section" means the duly numbered Section, with Clauses included in that Section, of these Regulations;*

kk. *"SGPA" means the Semester Grade Point Average as defined in the Academic Regulations;*

ll. *"Statutes" means the Statutes of Presidency University;*

mm. *"Sub-Clause" means the duly numbered Sub-Clause of these Program Regulations;*

nn. *"Summer Term" means an additional Academic Term conducted during the summer*

break (typically in June-July) for a duration of about eight (08) calendar weeks, with a minimum of thirty (30) University teaching days;

oo. "SWAYAM" means Study Webs of Active Learning for Young Aspiring Minds.

pp. "UGC" means University Grant Commission;

qq. "University" means Presidency University, Bengaluru; and

rr. "Vice Chancellor" means the Vice Chancellor of the University.

5. Program Description

The Master of Technology Degree Program Regulations and Curriculum 2024-2026 are subject to, and, pursuant to the Academic Regulations. These Program Regulations shall be applicable to the following ongoing Master of Technology (M.Tech.) Degree Programs of 2024-2026 offered by the Presidency School of Engineering (PSOE):

1. Master of Technology in Civil Engineering, abbreviated as M.Tech. (Civil Engineering)

2. Master of Technology in Embedded System and VLSI, abbreviated as M.Tech. (ESV)

3. Master of Technology in Mechanical Engineering, abbreviated as M.Tech. (Mechanical Engineering);

5.1 These Program Regulations shall be applicable to other similar programs, which may be introduced in future.

5.2 These Regulations may evolve and get amended or modified or changed through appropriate approvals from the Academic Council, from time to time, and shall be binding on all concerned.

5.3 The effect of periodic amendments or changes in the Program Regulations, on the students admitted in earlier years, shall be dealt with appropriately and carefully, so as to ensure that those students are not subjected to any unfair situation whatsoever, although they are required to conform to these revised Program Regulations, without any undue favour or considerations

6. Minimum and Maximum Duration

6.1 Master of Technology Degree Program is a Two-Year, Full-Time Semester based program. The minimum duration of the M.Tech. Program is two (02) years and each year comprises of two academic Semesters (Odd and Even Semesters) and hence the duration of the M.Tech. program is four (04) Semesters.

6.2 A student, who for whatever reason is not able to complete the Program within the normal period or the minimum duration (number of years) prescribed for the Program, may be allowed a period of two years beyond the normal period to complete the mandatory minimum credits requirement as prescribed by the concerned Program Regulations and Curriculum. In general, the permissible maximum duration (number of years) for completion of Program is 'N' + 2 years, where 'N' stands for the normal or minimum duration (number of years) for completion of the concerned Program as prescribed by the concerned Program Regulations and Curriculum.

6.3 The time taken by the student to improve Grades/CGPA, and in case of temporary withdrawal/re-joining (Refer to Clause **Error! Reference source not found.** of Academic Regulations), shall be counted in the permissible maximum duration for completion of a Program.

6.4 In exceptional circumstances, such as temporary withdrawal for medical exigencies where there is a prolonged hospitalization and/or treatment, as certified through hospital/medical records, women students requiring extended maternity break (certified by registered medical practitioner), and, outstanding sportspersons representing the University/State/India requiring extended time to participate in National/International sports events, a further extension of one (01) year may be granted on the approval of the Academic Council.

6.5 The enrolment of the student who fails to complete the mandatory requirements for the award of the concerned Degree (refer Section 19.**Error! Reference source not found.** of Academic Regulations) in the prescribed maximum duration (Sub-Clauses 18.1 and 18.2 of Academic Regulations), shall stand terminated and no Degree shall be awarded.

7 Programme Educational Objectives (PEO)

After four years of successful completion of the program, the graduates shall be able to:

PEO-1: Become successful professionals in industry, government, academia, research, entrepreneurial pursuit and consulting firms.

PEO-2: Contribute to society as broadly educated, expressive, ethical and responsible citizens with proven expertise

PEO-3: Achieve peer recognition as individuals or in a team through demonstration of good analytical, research, design and implementation skills.

PEO-4: Thrive to pursue life-long reflective learning to fulfill their goals.

8 Programme Outcomes (PO) and Programme Specific Outcomes (PSO)

8.1 Programme Outcomes (PO)

On successful completion of the Program, the students shall be able to:

PO1. Analyze, manage and supervise engineering systems and processes with the aid of appropriate advanced tools.

PO2. Design a system and process within constraints of health, safety, security, economics, and manufacturability to meet desired needs.

PO3. Carry out research in the respective discipline and publish the findings.

PO4. Effectively communicate and transfer the knowledge/ skill to stakeholders.

PO5. Realize the impact of engineering solutions in a contemporary, global, economical, environmental, and societal context for sustainable development.

8.2 Program Specific Outcomes (PSOs):

On successful completion of the Program, the students shall be able to:

PSO1: Become a successful engineer by applying the knowledge of Embedded System Design, Software for Embedded Systems, CMOS VLSI Design and Advanced Digital System Design.

PSO2: Evolve as a successful entrepreneur by understanding the impact of Embedded Systems and provide solutions to real world problems related to global, environmental and socio-economic context specially related to IOT

PSO3: Transform into a successful researcher by identifying, formulating and solving the security, Defence and VLSI Design related problems.

PSO4: Identify, formulate and solve the communication engineering problems from knowledge gained during the course to work in a team as well as to lead a team.

9 Admission Criteria (as per the concerned Statutory Body)

The University admissions shall be open to all persons irrespective of caste, class, creed, gender or nation. All admissions shall be made on the basis of merit in the qualifying examinations; provided that forty percent of the admissions in all Programs of the University shall be reserved for the students of Karnataka State and admissions shall be made through a Common Entrance Examination conducted by the State Government or its agency and seats shall be allotted as per the merit and reservation policy of the State Government from time to time**.** The admission criteria to the M.Tech. Program is listed in the following Sub-Clauses:

9.1 An applicant who has successfully completed B. Tech course from a recognized university of India or outside or from Senior Secondary Board or equivalent, constituted or recognized by the Union or by the State Government of that Country for the purpose of issue of qualifying certificate on successful completion of the course, may apply for and be admitted into the Program.

9.2 Provided further, the applicant must have taken Electronics / Electronics and Comminucation / VLSI subject, and, the applicant must have obtained a minimum of 45% of the total marks (40% in case of candidates belonging to the Reserved Category as classified by the Government of Karnataka) in these subjects taken together.

9.3 The applicant must have appeared for Karnataka PG-CET, or any other State-level Engineering Entrance Examinations.

9.4 Reservation for the SC / ST and other backward classes shall be made in accordance with the directives issued by the Government of Karnataka from time to time.

9.5 Admissions are offered to Foreign Nationals and Indians living abroad in accordance with the rules applicable for such admission, issued from time to time, by the Government of India.

9.6 Candidates must fulfil the medical standards required for admission as prescribed by the University.

9.7 If, at any time after admission, it is found that a candidate had not in fact fulfilled all the requirements stipulated in the offer of admission, in any form whatsoever, including possible misinformation and any other falsification, the Registrar shall report the matter to the Board of Management (BOM), recommending revoking the admission of the candidate.

9.8 The decision of the BOM regarding the admissions is final and binding.

10 Specific Regulations regarding Assessment and Evaluation (including the Assessment Details of NTCC Courses, Weightages of Continuous Assessment and End Term Examination for various Course Categories)

10.1 The academic performance evaluation of a student in a Course shall be according to the University Letter Grading System based on the class performance distribution in the Course.

10.2 Academic performance evaluation of every registered student in every Course registered by the student is carried out through various components of Assessments spread across the Semester. The nature of components of Continuous Assessments and the weightage given to each component of Continuous Assessments (refer clause 10.5 of academic regulations) shall be clearly defined in the Course Plan for every Course, and approved by the DAC.

10.3 Format of the End-Term examination shall be specified in the Course Plan.

10.4 Grading is the process of rewarding the students for their overall performance in each Course. The University follows the system of Relative Grading with statistical approach to classify the students based on the relative performance of the students registered in the concerned Course except in the following cases:

- Non-Teaching Credit Courses (NTCC)

Absolute grading method may be adopted, where necessary with prior approval of concerned DAC.

Grading shall be done at the end of the Academic Term by considering the aggregate performance of the student in all components of Assessments prescribed for the Course. Letter Grades (Clause **Error! Reference source not found.** of acedmic regulations) shall be awarded to a student based on her/his overall performance relative to the class performance distribution in the concerned Course. These Letter Grades not only indicate a qualitative assessment of the student's performance but also carry a quantitative (numeric) equivalent called the Grade Point.

10.5 Assessment Components and Weightage

Table 1: Assessment Components and Weightage for different category of Courses

Nature of Course and Structure	Evaluation Component	Weightage
Lecture-based Course L component in the L-T-P Structure is predominant (more than 1) (Examples: 3-0-0; 3-0-2; 2-1-0; 2-0-2, 2-0-4 etc.)	Continuous Assessments	50%
	End Term Examination	50%
Lab/Practice-based Course P component in the L-T-P Structure is predominant (Examples: 0-0-4; 1-0-4; 1-0-2; etc.)	Continuous Assessments	75%
	End Term Examination	25%

Skill based Courses like Industry Internship, Capstone project, Research Dissertation, Integrative Studio, Interdisciplinary Project, Summer / Short Internship, Social Engagement / Field Projects, Portfolio, and such similar Non-Teaching Credit Courses, where the pedagogy does not lend itself to a typical L-T-P structure	Guidelines for the assessment components for the various types of Courses, with recommended weightages, shall be specified in the concerned Program Regulations and Curriculum / Course Plans, as applicable.

The exact weightages of Evaluation Components shall be clearly specified in the concerned PRC and respective Course Plan.

Normally, for Practice/Skill based Courses, without a defined credit structure (L–T–P) [NTCC], but with assigned Credits (as defined in Clause **Error! Reference source not found.** of the Academic Regulations), the method of evaluation shall be based only on Continuous Assessments. The various components of Continuous Assessments, the distribution of weightage among such components, and the method of evaluation/assessment, shall be as decided and indicated in the Course Plan/PRC. The same shall be approved by the respective DAC.

10.6 Minimum Performance Criteria:

10.6.1 **Theory only Course and Lab/Practice Embedded Theory Course**

A student shall satisfy the following minimum performance criteria to be eligible to earn the credits towards the concerned Course:

a. A student must obtain a minimum of 30% of the total marks/weightage assigned to the End Term Examinations in the concerned Course.

b. The student must obtain a minimum of 40% of the AGGREGATE of the marks/weightage of the components of Continuous Assessments, Mid Term Examinations and End Term Examinations in the concerned Course.

10.6.2 **Lab/Practice only Course and Project Based Courses**

The student must obtain a minimum of 40% of the AGGREGATE of the marks/weightage of all assessment components in the concerned Course.

10.6.3 A student who fails to meet the minimum performance criteria listed above in a Course shall be declared as "Fail" and given "F" Grade in the concerned Course. For theory Courses, the student shall have to re-appear in the "Make-Up Examinations" as scheduled by the University in any subsequent semester, or, re-appear in the End Term Examinations of the same Course when it is scheduled at the end of the following Semester or Summer Term, if offered. The marks obtained in the Continuous Assessments (other than the End Term Examination) shall be carried forward and be included in computing the final grade, if the student secures the minimum requirements (as per sub-Clauses 10.6.1 and 10.6.2 of academic regulations) in the "Make-Up Examinations" of the concerned Course. Further, the student has an option to re-register for the Course

and clear the same in the summer term/ subsequent semester if he/she wishes to do so, provided the Course is offered.

11 Additional clarifications - Rules and Guidelines for Transfer of Credits from MOOC, etc. – Note: These are covered in Academic Regulations

The University allows students to acquire credits from other Indian or foreign institutions and/or Massive Open Online Course (MOOC) platforms, subject to prior approval. These credits may be transferred and counted toward fulfilling the minimum credit requirements for the award of a degree. The process of transfer of credits is governed by the following rules and guidelines:

11.1 The transfer of credits shall be examined and recommended by the Equivalence Committee (Refer **Error! Reference source not found.** of academic regulations) and approved by the Dean - Academics.

11.2 Students may earn credits from other Indian or foreign Universities/Institutions with which the University has an MOU, and that MOU shall have specific provisions, rules and guidelines for transfer of credits. These transferred credits shall be counted towards the minimum credit requirements for the award of the degree.

11.3 Students may earn credits by registering for Online Courses offered by *Study Web of Active Learning by Young and Aspiring Minds* (SWAYAM) and *National Program on Technology Enhanced Learning* (NPTEL), or other such recognized Bodies/ Universities/Institutions as approved by the concerned BOS and Academic Council from time to time. The concerned School/Parent Department shall publish/include the approved list of Courses and the rules and guidelines governing such transfer of credits of the concerned Program from time to time. The Rules and Guidelines for the transfer of credits specifically from the Online Courses conducted by SWAYAM/ NPTEL/ other approved MOOCs are as stated in the following Sub-Clauses:

11.3.1 A student may complete SWAYAM/NPTEL/other approved MOOCs as mentioned in Clause 11.3 (as per academic regulations) and transfer equivalent credits to partially or fully complete the mandatory credit requirements of Discipline Elective Courses and/or the mandatory credit requirements of Open Elective Courses as prescribed in the concerned Curriculum Structure. However, it is the sole responsibility of the student to complete the mandatory credit requirements of the Discipline Elective Courses and the Open Elective Courses as prescribed by the Curriculum Structure of the concerned Program.

11.3.2 SWAYAM/NPTEL/ other approved MOOCs as mentioned in Clause 11.3 (as per academic regulations) shall be approved by the concerned Board of Studies and placed (as Annexures) in the concerned PRC.

11.3.3 Parent Departments may release a list of SWAYAM/NPTEL/other approved MOOCs for Pre-Registration as per schedule in the Academic Calendar or through University Notification to this effect.

11.3.4 Students may Pre-Register for the SWAYAM/NPTEL/other approved MOOCs in the respective Departments and register for the same Courses as per

the schedule announced by respective Online Course Offering body/institute/ university.

11.3.5 A student shall request for transfer of credits only from such approved Courses as mentioned in Sub-Clause 11.3.2 above.

11.3.6 SWAYAM/NPTEL/other approved MOOCs Courses are considered for transfer of credits only if the concerned student has successfully completed the SWAYAM/NPTEL/other approved MOOCs and obtained a certificate of successful/satisfactory completion.

11.3.7 A student, who has successfully completed the approved SWAYAM/NPTEL / other approved MOOCs and wants to avail the provision of transfer of equivalent credits, must submit the original Certificate of Completion, or such similar authorized documents to the HOD concerned, with a written request for the transfer of the equivalent credits. On verification of the Certificates/Documents and approval by the HOD concerned, the Course(s) and equivalent Credits shall forwarded to the COE for processing of results of the concerned Academic Term.

11.3.8 The credit equivalence of the SWAYAM/NPTEL/other approved MOOCs are based on Course durations and/or as recommended by the Course offering body/institute/university. The Credit Equivalence mapped to SWAYAM/ NPTEL approved Courses based on Course durations for transfer of credits is summarised in Table shown below. The Grade will be calculated from the marks received by the Absolute Grading Table **Error! Reference source not found.** in the academic regulations.

Table 2: Durations and Credit Equivalence for Transfer of Credits from SWAYAM-NPTEL/ other approved MOOC Courses

Sl. No.	Course Duration	Credit Equivalence
1	4 Weeks	1 Credit
2	8 Weeks	2 Credits
3	12 Weeks	3 Credits

11.3.9 The maximum permissible number of credits that a student may request for credit transfer from MOOCs shall not exceed 20% of the mandatory minimum credit requirements specified by the concerned Program Regulations and Curriculum for the award of the concerned Degree.

11.3.10 The University shall not reimburse any fees/expense; a student may incur for the SWAYAM/NPTEL/other approved MOOCs.

11.4 The maximum number of credits that can be transferred by a student shall be limited to forty percent (40%) of the mandatory minimum credit requirements specified by the concerned Program Regulations and Curriculum for the award of the concerned Degree. However, the grades obtained in the Courses transferred from other Institutions/MOOCs, as mentioned in this Section (11.**Error! Reference source not found.**) shall not be included in the calculation of the CGPA.

12 Structure / Component with Credit Requirements Course Baskets & Minimum Basket wise Credit Requirements

The M.Tech. (Embedded System & VLSI) Program Structure (2024-2026) totalling 68 credits. Table 3 summarizes the type of baskets, number of courses under each basket and the associated credits that are mandatorily required for the completion of the Degree.

Table 3: M.Tech. (Embedded System & VLSI) 2024-2026: Summary of Mandatory Courses and Minimum Credit Contribution from various Baskets

Sl. No.	Baskets	Credit Contribution
1	School Core Courses (SC)	32
2	Program Core Courses (PC)	15
3	Discipline Elective Courses (DE)	15
4	Open Elective Courses (OEC)	06
	Total Credits	**68 (Minimum)**

In the entire Program, the practical and skill based course component contribute to an extent of approximately 51% out of the total credits of 68 for M.Tech. (Embedded System & VLSI) program of two years duration.

13 Minimum Total Credit Requirements of Award of Degree

As per the AICTE guidelines, a minimum of 68 credits is required for the award of an M.Tech. Degree.

14 Other Specific Requirements for Award of Degree, if any, as prescribed by the Statutory Bodies,

16.1 The award of the Degree shall be recommended by the Board of Examinations and approved by the Academic Council and Board of Management of the University**.**

16.2 A student shall be declared to be eligible for the award of the concerned Degree if she/he:

14.1 Fulfilled the Minimum Credit Requirements and the Minimum Credits requirements under various baskets;

14.2 Secure a minimum CGPA of 5.00 in the concerned Program at the end of the Semester/Academic Term in which she/he completes all the requirements for the award of the Degree as specified in Sub-Clause 14.1 of Academic Regulations**;**

14.3 No dues to the University, Departments, Hostels, Library, and any other such Centers/ Departments of the University; and

14.4 No disciplinary action is pending against her/him.

15 Structure – Basket Wise Course List (not Semester Wise)
List of Courses Tabled – aligned to the Program Structure
(Course Code, Course Name, Credit Structure (LTPC), Contact Hours, Course Basket, Type of Skills etc., as applicable).

Table 3.1 : School Core Courses (SC)						
S.No	Course Code	Course Name	L	T	P	C
1	MAT6001	Advanced Engineering Mathematics	3	0	0	3
2	ENG5001	English for Employability	2	0	2	3
3	SEM5001	Seminar – I	-	-	-	1
4	SEM5002	Seminar – II	-	-	-	1
5	PIP6001	Dissertation/ Internship - I	-	-	-	10
6	PIP6002	Dissertation/ Internship - II	-	-	-	14
		Total No. of Credits				**32**

Table 3.2 : List of Program Core Courses (PCC)						
S.No	Course Code	Course Name	L	T	P	C
1	ECE6001	Embedded System Design	2	0	2	3
2	ECE6002	CMOS VLSI Design	2	0	2	3
3	ECE5005	Advanced Digital System Design	3	0	0	3
4	ECE5006	Hardware Software Co-Design	3	0	0	3
5	ECE5007	Embedded Real Time Operating System	3	0	0	3
		Total No. of Credits				**15**

16 Practical / Skill based Courses – Internships / Thesis / Dissertation / Capstone Project Work / Portfolio / Mini project

Practical / Skill based Courses like internship, project work, capstone project, research project / dissertation, and such similar courses, where the pedagogy does not lend itself to a typical L-T-P-C Structure as defined in Clause 5.1 of the Academic Regulations, are simply assigned the number of Credits based on the quantum of work / effort required to fulfill the learning objectives and outcomes prescribed for the concerned Courses. Such courses are referred to as Non-Teaching Credit Courses (NTCC). These Courses are designed to provide students with hands-on experience and skills essential for their professional development. These courses aim to equip students with abilities in problem identification, root cause analysis, problem-solving, innovation, and design thinking through industry exposure and project-based learning. The expected outcomes are first level proficiency in problem solving and design thinking skills to better equip M.Tech. graduates for their professional careers. The method of evaluation and grading for the Practical / Skill based Courses shall be prescribed and approved by the concerned Departmental Academic Committee (refer Annexure A of the Academic Regulations). The same shall be prescribed in the Course Plan.

16.1 Internship

A student may undergo an Internship for a period of 12-14 weeks in an industry / company or academic / research institution during the 3rd Semester and 4th Semester, subject to the following conditions:

16.1.1 The Internship shall be in conducted in accordance with the Internship Policy prescribed by the University from time to time.

16.1.2 The selection criteria (minimum CGPA, pass in all Courses as on date, and any other qualifying criteria) as applicable / stipulated by the concerned Industry / Company or academic / research institution for award of the Internship to a student;

16.1.3 The number of Internships available for the concerned Academic Term. Further, the available number of internships shall be awarded to the students by the University on the basis of merit using the CGPA secured by the student. Provided further, the student fulfils the criteria, as applicable, specified by the Industry / Company or academic / research institution providing the Internship, as stated in Sub-Clause 16.1.2 above.

16.1.4 A student may opt for Internship in an Industry / Company or academic / research institution of her / his choice, subject to the condition that the concerned student takes the responsibility to arrange the Internship on her / his own. Provided further, that the Industry / Company or academic / research institution offering such Internship confirms to the University that the Internship shall be conducted in accordance with the Program Regulations and Internship Policy of the University.

16.1.5 A student selected for an Internship in an industry / company or academic / research institution shall adhere to all the rules and guidelines prescribed in the Internship Policy of the University.

16.2 Project Work

A student may undergo a Project Work for a period of 12-14 weeks in an industry / company or academic / research institution during the 3rd Semester and 4th Semester, subject to the following conditions:

16.2.1 The Project Work shall be approved by the concerned HOD and be carried out under the guidance of a faculty member.

16.2.2 The student may do the project work in an Industry / Company or academic / research institution of her / his choice subject to the above mentioned condition (Sub-Clause 2.6.2.1). Provided further, that the Industry / Company or academic / research institution offering such project work confirms to the University that the project work will be conducted in accordance with the Program Regulations and requirements of the University.

16.3 Capstone Project

A student may undergo a Capstone Project for a period of 12-14 weeks in an industry / company or academic / research institution in the 3rd Semester and 4th Semester as applicable, subject to the following conditions:

16.3.1 The Capstone Project shall be in conducted in accordance with the Capstone Project Policy prescribed by the University from time to time.

16.3.2 The selection criteria (minimum CGPA, pass in all Courses as on date, and any other qualifying criteria) as applicable / stipulated by the concerned Industry / Company or academic / research institution for award of the Capstone Project to a student;

16.3.3 The number of Capstone Project available for the concerned Academic Term. Further, the available number of Capstone Project shall be awarded to the students by the University on the basis of merit using the CGPA secured by the student. Provided further, the student fulfils the criteria, as applicable, specified by the Industry / Company or academic / research institution providing the Capstone Project, as stated in Sub-Clause 2.6.3.2 above.

16.3.4 A student may opt for Capstone Project in an Industry / Company or academic / research institution of her / his choice, subject to the condition that the concerned student takes the responsibility to arrange the I Capstone Project on her / his own. Provided further, that the Industry / Company or academic / research institution offering such Capstone Project confirms to the University that the Capstone Project shall be conducted in accordance with the Program Regulations and Internship Policy of the University.

16.3.5 A student selected for a Capstone Project in an industry / company or academic / research institution shall adhere to all the rules and guidelines prescribed in the Capstone Project Policy of the University.

16.4 Research Project / Dissertation

A student may opt to do a Research Project / Dissertation for a period of 12-14 weeks in an Industry / Company or academic / research institution or the University Department(s) as an equivalence of Internship, subject to the following conditions:

16.4.1 The Research Project / Dissertation shall be approved by the concerned HOD and be carried out under the guidance of a faculty member.

The student may do the Research Project / Dissertation in an Industry / Company or academic / research institution of her / his choice subject to the above mentioned condition (Sub-Clause 16.4.1). Provided further, that the Industry / Company or academic / research institution offering such Research Project / Dissertation confirms to

the University that the Research Project / Dissertation work will be conducted in accordance with the Program Regulations and requirements of the University.

17 List of Elective Courses under various Specialisations / Stream Basket

Table 3.3 : Discipline Elective Courses						
S. No.	Course Code	Course Name	L	T	P	C
General Basket						
1	ECE5008	Software for Embedded Systems	3	0	0	3
2	ECE5009	ASIC Design and Modelling	3	0	0	3
3	ECE5010	Design for Testability	3	0	0	3
4	ECE5011	CAD for VLSI	3	0	0	3
5	ECE5012	Reconfigurable Computing	3	0	0	3
6	ECE5013	VLSI Architecture	3	0	0	3
7	ECE5014	Networked Embedded Applications	3	0	0	3
8	ECE5015	Network Security	3	0	0	3
9	ECE5016	IC Fabrication Technology	3	0	0	3
10	ECE5017	Software Defined Radio	3	0	0	3
11	ECE5018	Memory Design	3	0	0	3
12	ECE6003	Low Power VLSI Design	3	0	0	3
13	ECE6004	Processor Design	3	0	0	3
14	ECE6005	Embedded Intelligence	3	0	0	3
15	ECE6006	VLSI Signal Processing	3	0	0	3

18 List of Open Electives to be offered by the School / Department (Separately for ODD and EVEN Semesters.

Table 3.8 : Open Elective Courses						
Sl. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**
Civil Engineering Basket						
1	CIV5001	Sustainable Smart Cities	3	0	0	3
2	CIV5002	Systems Design for Sustainability	3	0	0	3
3	CIV5003	Self-Sustainable Buildings	3	0	0	3
4	CIV5004	Energy and Buildings	3	0	0	3
Law Basket						
1	LAW5001	International Trade Law	3	0	0	3
2	LAW5002	Law relating to Business Establishment	3	0	0	3
3	LAW5003	Data Protection Law	3	0	0	3
4	LAW5004	Law Relating to Consumer Protection	3	0	0	3
5	LAW5005	Law Relating to Infrastructure Projects	3	0	0	3
Computer Science Basket						
1	CSE5001	Programming Methodologies using Java	2	0	0	2
2	CSE5002	Human Computer Interaction	0	0	2	1
3	CSE5003	IOT Applications	2	0	0	1
4	CSE5004	Programming Essentials in Python	0	0	2	2
5	CSE2003	Social Network Analytics	3	0	0	3
Electronics and Communication Engineering Basket						
1	ECE5001	Wearable Computing	3	0	0	3
2	ECE5002	MEMS and Nanotechnology	3	0	0	3
3	ECE5003	Advanced Computer Networks	3	0	0	3

4	ECE5004	Pervasive Computing	3	0	0	3
Mechanical Engineering Basket						
1	MEC5001	Optimization Techniques	3	0	0	3
2	MEC5002	Industry 4.0	3	0	0	3
3	MEC5003	Six Sigma for Engineers	3	0	0	3
4	MEC5004	Design for Internet of Things	3	0	0	3
Management Basket						
1	MBA3042	Innovation and Business Incubation	3	0	0	3
2	MBA3037	Personal Wealth Management	3	0	0	3
3	MBA3038	Team Dynamics	3	0	0	3
4	MBA3039	Market Research	3	0	0	3
5	MBA2023	Design Thinking for Business Innovation	3	0	0	3
6	MBA3046	Game Theory in Business	3	0	0	3
7	MBA3047	Data Story Telling	3	0	0	3
8	MBA3048	Environmental Sustainability and Value Creation	3	0	0	3
9	MBA3049	Industry 4.0	3	0	0	3
Media Studies Basket						
1	BAJ5001	Media and Entertainment Business	3	0	0	3
2	BAJ5002	TV Journalism and News Management	2	0	2	3
Research Basket						
1	RES5001	Research Methodology	3	0	0	3
2	RES3001	Research Methodology	3	0	0	3
Research Project Basket						
1	URE7001	University Research Experience	-	-	-	3
	URE7002	University Research Experience	-	-	-	3

19 List of MOOC (NPTEL) Courses

19.1 NPTEL - Discipline Elective Courses for M. Tech. (Electronics and Communication Engineering)

Sl. No.	Course ID	Course Name	Duration
1	noc25-cs22	Deep Learning for Natural Language Processing	12 Weeks
2	noc25-ee13	Computer Vision And Image Processing - Fundamentals And Applications	12 Weeks
3	noc25-ee25	Digital VLSI Testing	12 Weeks
4	noc25-ee31	Embedded Sensing, Actuation and Interfacing Systems	12 Weeks
5	noc25-ee58	Optical Fiber Sensors	12 Weeks
6	noc25-ee62	Physics of Nanoscale Devices	12 Weeks
7	noc25-ee73	RF Transceiver Design	12 Weeks
8	noc25-ee79	Smart Grid: Basics to Advanced Technologies	12 Weeks
9	noc25-ee83	VLSI Physical Design with Timing Analysis	12 Weeks
10	noc25-ee75	Semiconductor Devices for Next Generation Field Effect Transistors (More than Moore): A Physics Perspective	12 Weeks

19.2 NPTEL - Open Elective Courses for M. Tech. (Electronics and Communication Engineering)

Sl. No.	Course ID	Course Name	Duration
1	noc25-cs04	Affective Computing	12 Weeks
2	noc25-cs08	Blockchain and its Applications	12 Weeks
3	noc25-cs11	Cloud Computing	12 Weeks
4	noc25-cs32	Foundations of Cyber Physical Systems	12 Weeks
5	noc25-cs38	Human Computer Interaction (In English)	12 Weeks
6	noc25-cs51	Natural Language Processing	12 Weeks
7	noc25-cs45	Introduction to Large Language Models (LLMs)	12 Weeks
8	noc25-cs02	Advanced Computer Networks	12 Weeks
9	noc25-cs70	Theory of Computation	12 Weeks

20 Recommended Semester Wise Course Structure / Flow including the Programme / Discipline Elective Paths / Options

Semester 1										
S. NO.	COURSE CODE	COURSE NAME	CREDIT STRUCTURE					BASKET	TYPE OF SKILL	COURSE ADDRESSES TO
			L	T	P	C	CONTACT HOURS			
1	MAT6001	Advanced Engineering Mathematics	3	0	0	3	3	SC	S	
2	ENG5001	English for Employability	2	0	2	3	4	SC	S	HP
3	ECE6001	Embedded System Design	2	0	2	3	4	PC	F / S / EM / EN	HP/ ES
4	ECE6002	CMOS VLSI Design	2	0	2	3	4	PC	F / S / EM / EN	HP/ ES
5	ECE5005	Advanced Digital System Design	3	0	0	3	3	PC	S / EM	HP
6	ECEXXXX	Discipline Elective - I	3	0	0	3	3	DE		
7	ECEXXXX	Discipline Elective - II	3	0	0	3	3	DE		
8	SEM5001	Seminar – I	-	-	-	1	0	SC	S/EM	
		TOTAL				22	21	-	-	-

Semester 2										
S. NO.	COURSE CODE	COURSE NAME	CREDIT STRUCTURE					BASKET	TYPE OF SKILL	COURSE ADDRESSES TO
			L	T	P	C	CONTACT HOURS			
1	ECE5006	Hardware Software Co-Design	3	0	0	3	3	PC	S / EM	HP
2	ECE5007	Embedded Real Time Operating System	3	0	0	3	3	PC	F / S / EM	HP
3	ECE XXXX	Discipline Elective – III	3	0	0	3	3	DE		
4	ECE XXXX	Discipline Elective – IV	3	0	0	3	3	DE		
5	ECE XXXX	Discipline Elective - V	3	0	0	3	3	DE		
6	XXX XXXX	Open Elective - I	3	0	0	3	3	OE		
7	XXX XXXX	Open Elective - II	3	0	0	3	3	OE		
8	SEM5002	Seminar – II	-	-	-	1	0	SC	S/EM	
		TOTAL				22	21			

Semester 3										
S. NO.	**COURSE CODE**	**COURSE NAME**	**CREDIT STRUCTURE**					**BASKET**	**TYPE OF SKILL**	**COURSE ADDRESSES TO**
			L	**T**	**P**	**C**	**CONTACT HOURS**			
1	PIP6001	Dissertation/ Internship - I	-	-	-	10	-	SC	S/ EM/ EN	HP/ ES
		TOTAL				10	-			

Semester 4										
S. NO.	**COURSE CODE**	**COURSE NAME**	**CREDIT STRUCTURE**					**BASKET**	**TYPE OF SKILL**	**COURSE ADDRESSES TO**
			L	**T**	**P**	**C**	**CONTACT HOURS**			
1	PIP6002	Dissertation/ Internship - II	-	-	-	14	-	SC	S/ EM/ EN	HP/ ES
		TOTAL				14	-			

21 Course Catalogue

Course Catalogue of all Courses Listed including the Courses Offered by other School / Department and Discipline / Programme Electives – Course Code, Course Name, Prerequisite, Anti-requisite, Course Description, Course Outcome, Course Content (with Blooms Level, CO, No. of Contact Hours), Reference Resources.

The Course Catalogues for the Courses offered in each basket are attached below after the Semester wise grids:

Course Code: ECE6001	Course Title: Embedded System Design Type of Course: Theory and Lab Integrated	L-T-P-C	2	0	2	3
Version No.	2.0					
Course Pre-requisites	Microprocessor and Microcontroller					
Anti-requisites	NIL					
Course Description	The focus of this course will be to discuss the Embedded Systems and their design using ARM microcontrollers. System design examples and case studies for real-world applications will be undertaken. This course will be duly supported by a laboratory component under which real-time interfacing of sensors, microcontrollers and actuators will be covered.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of Embedded System Design and attain SKILL DEVELOPMENT through EXPERIENTIAL LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: 1. Select Embedded Systems and the components needed to develop such systems. 2. Distinguish various ARM architecture versions and processors. 3. Program ARM processors using Assembly Language and C Languages. 4. Interface various on-chip as well as off-chip peripherals to develop embedded applications. 5. Develop Embedded C programs for various real world applications					
Course Content:						
Module 1	Fundamentals of Embedded Systems	Quiz	Memory Recall based Quizzes		06 session	
Topics: Introduction to Embedded Systems, Applications of Embedded and Research Areas of Embedded Systems, Hardware and Software in Embedded Systems, Classifications of Embedded Systems, Design Challenges, Metrics, Processors in Embedded Systems. RISC and CISC Architectures. Memories, Exemplary Embedded Systems I/O Devices, Software in Embedded Systems, Device Driver Concepts, Design Methodology.						

Module 2	ARM Architecture	Assignment / Quiz	Programming and Simulation task / Memory Recall based Quizzes	06 session
Topics: Introduction to ARM® Architecture and ARM® Cortex™-M TM4C123X processor, Comparing ARM® Cortex™-M TM4C123X processor with TM4C129X architecture, ARM and Thumb Instruction Set Overview and Addressing Modes.				
Module 3	ARM Programming	Assignment	Programming Assignment	10 session
Topics: Review of ARM Addressing Modes, ARM Assembly Programming, Concepts of Input and Output Ports, Basics of Interfacing Switches and LEDs, Basic Concepts of Modular Programming, Programming ARM Controllers using C – Conditional Statements, Loop Statements, debugging, single stepping, breakpoints, pointers and data structures, variables, numbers and parameter passing, Introduction to RTOS on ARM.				
Module 4	Interfacing Peripherals with ARM Processors	Assignment	Interfacing and Programming Assignment	08 session
Topics: TM4C123X / TM4C129X Timers, Pulse Width Modulation, Interfacing Stepper Motors and DC Motors, Serial Communication, TM4C123X / TM4C129X UARTs, Analog I/O Interfacing, TM4C123X / TM4C129X ADCs and DACs, General Purpose Processor based Design, I2Cs and CANs on TM4C123X / TM4C129X, Embedded System Hardware and Software Design Issues.				
List of Laboratory Tasks: Exp 01:- Level 01-WAP to find addition/Subtraction of two 32-bit numbers. Level 02 -WAP to find average of 'n' 32-bit numbers. Exp 02:- Level 01-WAP to find multiplication and Divison of two 32-bit numbers. Level 02-WAP to transfer a block of word from Source to destination memory Exp 03:- Level 01-WAP to find multiplication and Divison of two 32-bit numbers. Level 02-WAP to transfer a block of word from Source to destination memory Exp 04:- Level 01- WAP to implement hexadecimal addition/ subtraction. Level 02- WAP to implement hexadecimal multiplication Exp 05:- Level 01-CCS IDE with C-Programming Level 02- Interfacing of ARM with basic Input / Output Devices LEDs Exp 06:- Interfacing of ARM with basic Input / Output Devices switches Exp 07:-Interfacing of ARM with basic Input / Output Devices PUSH Button Exp 08:- Pulse Width Modulation (PWM) based Waveform Generation and Timing using ARM				

Exp 09:- Interfacing of Analog-to-Digital (ADC) and Digital-to-Analog (DAC) Converters with ARM

Exp 10:- Interfacing of Sensors (Temperature Sensors / Ultrasonic Sensors etc.) with ARM • Integrating multiple devices in a small project

Exp 11:- Interfacing of Displays (LCDs / seven-segment LEDs etc.) with ARM

Targeted Application & Tools that can be used:

Targeted Applications: Industry 4.0, Biomedical and Agricultural automation

Professionally Used Software: Keil Version 05/ Code Composer Studio

Project Work/Assignment:

1. Case Study: At the end of the course students will be given a 'real-world' application-based on real world embedded system case study. Students will be submitting a report which will include Application Design, sensors used, middleware protocols used and working mechanism etc. in appropriate format

2 Book/Article review: At the end of the course a literature review of any 05 recent articles from the reputed national and international journal/ conferences will be given by students. They need to refer to tools like Scopus/ Google-Scholar and submit a report on their understanding of the assigned article in appropriate format.

3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to present their review work.

Text Book(s):

1. Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide, Designing and Optimizing System Software", Morgan Kaufmann Publishers, 2nd Edition.
2. Alexander G. Dean, "Embedded Systems Fundamentals with Arm Cortex M Based Microcontrollers: A Practical Approach", ARM Education Media, 2nd Edition

Reference(s):

Reference Book(s):

1. Jonathan W. Valvano, "Embedded Systems: Introduction to Arm® Cortex™-M Microcontroller- Vol 01", CreateSpace Independent Publishing Platform, 1st Edition
2. Jonathan W. Valvano, "Embedded Systems: Real-Time Operating Systems for Arm® Cortex™-M Microcontrollers", CreateSpace Independent Publishing Platform, 1st Edition.
3. ARM Cortex Datasheet available on (https://www.arm.com/)

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Free online self-paced course :- https://bcourses.berkeley.edu.
2. Online notes :- https://mitpress.mit.edu/books/internet-things
3. NPTEL online video content:- http://www.digimat.in/nptel/courses/video/106105160/L22.html
4. Online ppts :- https://www.upf.edu/pra/en/3376/22580
5. Online ppts:- https://www.macs.hw.ac.uk/~dwcorne/Teaching/introdl.ppt

E-content:

1. Joseph Sifakis, " Embedded systems design - Scientific challenges and work directions 2009 Design, Automation & Test in Europe Conference & Exhibition https://ieeexplore.ieee.org/document/5090623

2. Gabor Karsai; Fabio Massacci; Leon Osterweil; Ina Schieferdecker," Evolving

Embedded Systems", Computer , VOL. 43, issue.5
https://ieeexplore.ieee.org/document/5472888

3. Sachin P. Kamat," An eye on design: Effective embedded system software", IEEE Potentials, VOL. 29, issue.5
https://ieeexplore.ieee.org/document/5568178

4. Ahmed Abdallah; Eric M. Feron; Graham Hellestrand; Philip Koopman; Marilyn Wolf, " Hardware/Software Codesign of Aerospace and Automotive Systems", Proceedings of the IEEE , VOL. 98, issue.4
https://ieeexplore.ieee.org/document/5440056

Topics relevant to "SKILL DEVELOPMENT": Classifications of Embedded Systems, Design Challenges, Metrics, Processors in Embedded Systems. RISC and CISC Architectures for developing SKILL DEVELOPMENT through

EXPERIENTIAL LEARNING. This is attained through assessment component mentioned in course plan.

Catalogue prepared by	Mr. Kiran Dhanaji Kale
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18, Dated 03/08/2022

Course Code: ECE6002	Course Title: CMOS VLSI DESIGN Type of Course: Theory integrated Lab	L-T- P- C	2	0	2	3
Version No.	2.0					
Course Pre-requisites	Basic concepts of circuit design that involves diode and Transistor with their interconnections and current and voltage levels. Basics of logic gates and transistor level implementation of Digital Logic Circuits such as logic gates, MSI, LSI combinational circuits and sequential circuits.					
Anti-requisites	NIL					
Course Description	This course introduces the design and implementation of VLSI circuits for complex digital and analog applications. The course starts with basic understanding of transistor level device modeling to the complex digital circuits based on the current trends of IC technology. The associated laboratory provides an opportunity to develop the transistor level circuit design and validate the developed concepts in real time using the EDA tools. This lab practice could enhance the learner's ability to visualize the real-world problems to derive solutions.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of CMOS VLSI DESIGN and attain SKILL DEVELOPMENT through Experiential Learning.					
Course Outcomes	On successful completion of this course the students shall be able to: 1. Discuss the basics of VLSI design and understand the basic VLSI design flow, process flow and design methodologies. 2. Interpret the MOS transistor theory and various ideal and non-ideal characteristics of MOS transistors. 3. Develop combinational and sequential circuits using Hardware Description Language and various design parameters of digital circuits using cadence tool 4. Interpret Memory elements along with timing considerations and testing and testability issues in VLSI Design					
Course Content:						
Module 1	Introduction to VLSI systems & MOSFET Design Process	Assignment	Designing and Analysis task		9 Sessions	
Topics: Introduction to IC Technology, Types of Integrated Circuits, Overview of VLSI design methodologies, Design domains – Y Chart, VLSI design flow, Fabrication Processes Flow – Basic Concepts, CMOS n-Well Process and Stick Diagrams – NMOS and CMOS design style.						
Module 2	MOS Transistor Theory	Assignment	Design Analysis		9 Sessions	
The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor (MOSFET), MOSFET Current-Voltage Characteristics, Non-Ideal I-V Effects, Channel Length Modulation and Threshold Voltage and MOSFET Scaling						
Module 3	Analog CMOS	Assignment	Design Analysis		7 Sessions	

	Design			
Introduction to Analog VLSI Design, MOSFET as a Switch and MOS Diode/Resistor, Common Source (CS) Amplifier with resistive, diode-connected load, Source follower (CD) Amplifier, Common Gate (CG) Amplifier.				
Module 4	CMOS Digital Design Semiconductor Memories	Assignment/Project	Simulation & Analysis	8 Sessions
Digital CMOS Design: CMOS Logic Circuits: Complex Logic Circuits ,CMOS Transmission Logic ,Complementary Pass-Transistor Logic ,Dynamic CMOS Logic ,Domino CMOS Logic Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory Testing and Verification: Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability.				
List of Laboratory Tasks: Experiment No 1: Basic Logic Gates. Level 1: Write the Verilog code for AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates using dataflow model and obtain the simulation waveforms. Level 2: Implement all the logic gates in Switch level modeling using Xilinx Tool. Experiment No 2: Half Adder, Full Adder Level 1: Write a Verilog code for Half Adder and Full Adder using behavioral modeling and obtain the simulation results. Level 2: Design a full adder using half adder and basic gates and verify the simulation results using Xilinx Tool. Experiment No 3: Multiplexer, De-multiplexer and Decoder Level 1: Write a Verilog code to design a 4:1 Multiplexer, 1:4 De-multiplexers and 3:8 Decoders and verify the simulation results for all possible input combinations. Level 2: Construct an 8:1 Multiplexer using a 2:1 multiplexer using a Verilog programming using Xilinx Tool. Experiment No 4: SR, JK, D & T Flip Flops Level 1: Write a Verilog code to design SR, JK and Flip flops and obtain the simulation results Level 2: Write a Verilog code to design T and D Flip flops using JK Flip flop and obtain the simulation results using Xilinx Tool.				

Experiment No 5: Measurement of Parameters of an Inverter

Level 1: Create the symbol of the inverter circuit and also perform the transient analysis of an inverter using Cadence Tool.

Level 2: Perform the DC analysis of an inverter to determine the delay time, rise time, fall time and power dissipation of an inverter using Cadence Tool.

Experiment No 6: CMOS NAND and NOR Gates

Level 1: Draw the CMOS schematic of the 2 input NAND and NOR gate, also draw the layout of the same, and simulate for transient result using Cadence Tool.

Level 2: Perform DC analysis to calculate Power and Delay of 2 input NAND and NOR Gate using Cadence Tool.

Experiment No 7: Common Source (CS), Common Drain (CD) and Common Gate (CG) Amplifier

Level 1: Carry out transient analysis, DC operating point and AC analysis of Common Drain (CD) and Common Gate (CG) Amplifier using Cadence Tool.

Level 2: Design a common source (CS) amplifier with and without resistive load using an n MOS transistor with a small-signal gain of at least 3 using Cadence Tool.

Experiment No 8: Layout of CMOS Inverter, NAND and NOR Gate

Level 1: Draw the layout of CMOS Inverter & perform LVS and QRC check using Cadence Tool.

Level 2: Draw the layout of CMOS NAND gate & perform LVS and QRC check using Cadence Tool.

Targeted Application & Tools that can be used:

Application Area is high-performance digital systems, such as microprocessors, digital signal processors (DSPs).

Professionally Used Software: Xilinx-ISE; VIVADO; Cadence-Virtuoso.

Open source tools: EDA Playground; LT-Spice; Micro wind.

Project work/Assignment:

1. Case Studies: At the end of the course students will be given a topic related to CMOS VLSI Design that would have been published, as a case study. Students will be submitting a report in appropriate format.

2. Book/Article review: At the end of each module a book reference or an article topic will be given to each student. They need to visit the library and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link .

3. Presentation: There will be a group presentation, where the students will be given a small signal model of CS AMPLIFIER. They will have to explain/demonstrate the working and discuss the applications for the same.

4. Assignments:

Project 1. Solving the numerical on process parameters of MOSFET like work function, threshold voltage.

Project 2. Draw transistor-level schematic of a CMOS complex logic gate that realizes (a) the function and (b) draw stick diagram of the same complex logic gate.

Textbook(s):

1. N. H. E. Weste, D. M. Harris, "CMOS VLSI Design". Fourth Edition, 2015 Pearson Education.
2. Sung Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", 3rd Edition, 2003,McGraw- Hill.

References:

Reference Book(s):

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India.
2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design" (original Edition – 1994), PHI 3rd Edition.
3. R. Jacob Baker, Harry W. Li., David E. Boyce, "CMOS: Circuit Design, Layout and Simulation",, 2003, PHI.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Lecture videos for CMOS Digital VLSI Design by Prof. Sudeb Dasgupta Department of Electrical Engineering, IIT Roorkre -- https://nptel.ac.in/courses/108107129
2. Video lectures on "VLSI Devices: Modeling and Simulation" by Prof. Dr. S K Lahiri, IIT KGP http://www.satishkashyap.com/2013/07/video-lectures-on-vlsi-devices-modeling.html .
3. PPT on Low Power VLSI Design, Link: http://www.engppt.com/2011/12/cmos-vlsi-design-methodologies.html

E-content:

1. M. Chanda, S. Jain, S. De and C. K. Sarkar, "Implementation of Subthreshold Adiabatic Logic for Ultralow-Power Application," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. .23, no. 12, pp. 2782-2790, Dec. 2015. https://ieeexplore.ieee.org/document/7018053
2. R. Raut and O. Ghasemi, "A power efficient wide band trans-impedance amplifier in sub-micron CMOS integrated circuit technology," *2008 Joint 6th International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference*, 2008, pp. 113-116, doi: 0.1109/NEWCAS.2008.4606334. https://ieeexplore.ieee.org/document/4606334
3. Badawy, Wael, and Magdy Bayoumi. "Low power VLSI architecture for 2D-mesh video object motion tracking." In *Proceedings IEEE Computer Society Workshop on VLSI 2000. System Design for a System-on-Chip Era*, pp. 67-72. IEEE, 2000. https://ieeexplore.ieee.org/abstract/document/844532
4. Badawy, Wael, and Magdy Bayoumi. "Low power VLSI architecture for 2D-mesh video object motion tracking." In *Proceedings IEEE Computer Society*

Workshop on VLSI 2000. System Design for a System-on-Chip Era, pp. 67-72. IEEE, 2000. https://ieeexplore.ieee.org/abstract/document/844532	
Topics relevant to "SKILL Development": World of wearables - VLSI Design Methodology, Power dissipation in Digital Integrated circuits for developing SKILL DEVELOPMENT through Experiential Learning. This is attained through assessment component mentioned in course handout	
Catalogue prepared by	Mrs. Srilakshmi K H
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18, Dated 03/08/2022

Course Code: ECE5005	Course Title: ADVANCED DIGITAL SYSTEM DESIGN Type of Course: Theory Only		L- T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Basic concepts of digital circuits like gates, flip-flops, registers, multiplexers, decoders etc.					
Anti-requisites	NIL					
Course Description	The focus of this course is to enable the students to Design the synchronous and Asynchronous Digital Systems through the study of ASM & FSM charts, Hardware description language coding, Reduction and assignments of state tables. Further, it elaborates the Test Generation and Fault diagnosis of Combinational circuits by conventional methods. It introduces various methods to analyze sequential circuits. Further it elaborated the circuit design using programmable devices. This course emphasizes Fault detection and diagnosis of Advanced digital electronic circuits.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of ADVANCED DIGITAL SYSTEM DESIGN and attain SKILL DEVELOPMENT through PARTICPATIVE LEARNING.					
Course Outcomes	On successful completion of the course the students shall be able to: CO1: Summarize the minimization theories of Sequential Machines. CO2: Discover the sequential circuit using programmable devices. CO3: Practice the techniques for fault modeling of digital systems. CO4: Illustrate the various Fault diagnosis algorithm					
Course Content:						
Module 1	Minimization and Transformation of Sequential Machines:	Assignment	Memory Recall based Quizzes	10 *Sessions*		
The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.						
Module 2	Advanced Digital Design and SM Charts:	Assignment/mini project	Memory Recall based Quizzes	10 *Sessions*		
Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, shift and add multiplier, Binary divider. - State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.						
Module 3	Fault Modeling	Assignment/mini project	Programing / simulation	11 *Sessions*		
Logic Fault model – Fault detection & Redundancy Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.						

Module 4	Fault diagnosis	Assignment/mini project	Programing / simulation	11 *Sessions*

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

Targeted Application & Tools that can be used:

This course is contributed for placement in data science companies, research & development work and also useful to know the existing & developing Artificial Intelligence.

Professionally Used Software: HDL (VHDL/ Verilog HDL)/ C++ / MatLab, Phython

Text Books:

1. N. N. Biswas, "*Logic Design Theory*", PHI, 2009. ISBN:9780135243985, 013524398X the University of Michigan- Prentice Hall
2. Zvi Kohavi , "*Switching and Finite Automata Theory*", TMH, 2nd Edition, 2005.
3. Norman Balabanian, Bradley Carlson, "*Digital Logic Design Principles*" Wiley Student Edition, 2007.

Reference Books

1. M. Abramovici, Melnin Breuer, Arthur Friedman, "*Digital System Testing and Testable Design*", Jaico Publications, Reprint Edition, 2008.
2. Charles H. Roth Jr., "*Fundamentals of Logic Design*", Cengage learning, 6th Edition, 2004.
3. Frederick. J. Hill & Peterson, "*Computer Aided Logic Design*", Wiley 4th Edition, 1993.

Online Resources (e-books, notes, ppts, video lectures etc)

1. State Minimization in synchronous sequential circuits - YouTube
2. Sequence detector 1100 || sequence detector 1101 overlapping mealy FSM - YouTube
3. Ebook1: Find PDF Logic Design Theory (colorado.edu)
4. Ebook2: Digital Systems Design | Download book (freebookcentre.net)
5. Nptel Digital System Design - Course (nptel.ac.in)
6. NPTEL :: Electrical Engineering - NOC:Digital System Design
7. https://www.researchgate.net/publication/348235247_Advanced_Digital_System_Design_-_A_Practical_Guide_to_Verilog_Based_FPGA_and_ASIC_Implementation/link/5ff4764d92851c13feefa0d2/download
8. https://www.researchgate.net/publication/3897013_Fault_Equivalence_Identification_Using_Redundancy_Information_and_Static_and_Dynamic_Extraction
9. http://www.pld.ttu.ee/diagnostika/theory/fault.html

Topics relevant to "Skill development": Machine Minimization

For developing Skill development" through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. G MUTHUPANDI
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18, Dated 03/08/2022

Course Code: ECE5006	Course Title: Hardware Software Codesign Type of Course: Theory only		L-T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Digital Electronics, System Design, Embedded Design and Development Systems, Basic C Programming.					
Anti-requisites	NIL					
Course Description	The course will begin by discussing the concepts, techniques and issues for co-design of hardware and software systems. The other important topics include co-synthesis algorithms, prototyping and emulation, processor architectures, compilation techniques and tools for a target processor architecture, design specification and verification for concurrent systems, heterogeneous architectures and use of integrated design tools.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of Hardware Software Codesign and attain SKILL DEVELOPMENT through PARTICPATIVE LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: 1. Acquire the knowledge about system specification and modeling. 2. Learn the formulation of partitioning the hardware and software 3. Analyze about the hardware and software integration 4. Formulate the design specification and module creation.					
Course Content:						
Module 1	Issues in Co-design	Quiz	Memory Recall based Quizzes	9 session		
Topics: Models and Architectures, Finite-State Machine with Data path, Languages, Concurrency, State Transitions, A Generic Co-Design Methodology, System Specification, Allocation and Partitioning, Scheduling. Communication synthesis, analysis and validation flow.						
Module 2	Algorithms, Prototyping and Emulation	Assignment / Quiz	Programming and Simulation task / Memory Recall based Quizzes	10 session		
Topics: Architectural Models, Performance Estimation, An Integer Linear Programming Model, Performance Analysis, Heuristic Algorithms, The Weaver Prototyping Environment, Quickturn Emulation Systems, Mentor SimExpress Emulation System, Zycad Paradigm RP and XP, Aptix Prototyping System, Arkos (Synopsys) and CoBalt (Quickturn) Emulation Systems						
Module 3	Architectures, Compilation Techniques and Tools	Assignment	Programming Assignment	10 session		

Topics:

Component specialization techniques, System Specialization, System Specialization Techniques, Memory Architectures, Communication Infrastructure, Application System Classes, Integration Leads to Processors, Architectures in Multimedia, Wireless, and Telecommunications, Examples of Emerging Architectures, Commercial Support of Embedded Processors, Compilation Technologies, compiler validation.

Module 4	Design Specification and Design	Group Discussion/Case Study	Interfacing and Programming Assignment	11 session

Topics:

Design, Co-design, language oriented intermediate forms, architecture oriented intermediate forms. distributed intermediate forms, The Plethora of System Specification languages, Comparing Specification Languages, Heterogeneous Specification and Multi-language Co-simulation, Automatic Generation of Co-Simulation Interfaces, Towards System Level Multi-language Specification and Co-Simulation

Targeted Application & Tools that can be used:

Targeted Applications: Industry 4.0, Automotive automation.

Professionally Used Software: Vivado Design Suite/ Software development kit.

Text Book(s):

T1. Jorgen Staunstrup, Wayne Wolf , "Hardware / Software Co- Design Principles and Practice," Springer.

Reference(s):

Reference Book(s):

1. Giovanni De Micheli, Mariagiovanna Sami, "Hardware / Software Co- Design," Kluwer Academic Publishers
2. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design," Springer
3. Class Notes (CN)

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Free online self-paced course: - http://courses.eees.dei.unibo.it/LABMPHSENG/course-info/.
2. Online notes :- https://cseweb.ucsd.edu/classes/wi17/cse237A-a/handouts/10.hwsw.pdf
3. NPTEL online video content:- http://www.digimat.in/nptel/courses/video/1061051623/L22.html
4. Online ppts :- https://www.upf.edu/pra/en/3376/22580
5. Online ppts:- www.powershow.com/view/12140f
6. Youtube Video:- https://www.youtube.com/watch?v=OJRBbOoiHXw

Presidency Library Link:

https://presiuniv.knimbus.com/user#/home

E-content:

1. Alok Prakash, Christopher T. Clarke, Siew-Kei Lam, Thambipillai Srikanthan, "Rapid Memory-Aware Selection of Hardware Accelerators in Programmable SoC Design", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.26, no.3, pp.445-456, 2014. https://ieeexplore.ieee.org/document/7450436/
2. Ayat, Sayed Omid, Mohamed Khalil-Hani, and Rabia Bakhteri. "OpenCL-based hardware-software co-design methodology for image processing implementation on heterogeneous FPGA platform." In *2015 IEEE International Conference on Control System, Computing and Engineering (ICCSCE)*, pp. 36-41. IEEE, 2015. https://ieeexplore.ieee.org/document/7482154

3. Jelemenská, Katarína, Martin Kardos, and Pavel Cicak. "HSSL specification high-level synthesis." In *2015 13th International Conference on Emerging eLearning Technologies and Applications (ICETA)*, pp. 1-6. IEEE, 2015. https://ieeexplore.ieee.org/document/7558479

4. Alhammami, Muhammad, Ooi Chee Pun, and Tan Wooi Haw. "Hardware/software co-design for accelerating human action recognition." In *2015 IEEE Conference on Sustainable Utilization And Development In Engineering and Technology (CSUDET)*, pp. 1-5. IEEE, 2015. https://ieeexplore.ieee.org/document/7446226

Topics relevant to "Skill development": Finite-State Machine with Data path, Languages, Concurrency, State Transitions, A Generic Co-Design Methodology, System Specification, Allocation and Partitioning, Scheduling For developing Skill development" through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Mr. V V S Vijaya Krishna
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18, Dated 03/08/2022

Course Code: ECE5007	Course Title: Embedded Real Time Operating Systems Type of Course: Theory only		L-T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Embedded System Design. Embedded C Programming, Basic Concepts of Operating Systems					
Anti-requisites	NIL					
Course Description	The objective of the course is to introduce the principles of real-time operating systems, and their use in the development of embedded multitasking application software. This course covers the principles of real-time systems, Task assignment and scheduling, Resource management, Real-time operating systems, RTOS services, Inter task communication, Case studies of real-time systems.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of real time operating systems and attain EMPLOYABILITY SKILLS through PARTICPATIVE LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: 1) Recognize and classify embedded and real-time systems 2) Classify and exemplify scheduling algorithms 3) Learn various approaches to real-time scheduling 4) Learn software development process and tools for RTOS applications					
Course Content:						
Module 1	Introduction to RTOS	Quiz	Memory Recall based Quizzes	09 session		
Topics: Introduction to Embedded Real Time Operating Systems (RTOS), Need of RTOS, Characteristics of RTOS Structure of a Real Time System, Architecture of Kernel, Hardware Considerations: logic states, CPU, memory, I/O						
Module 2	Real Time Scheduling	Assignment / Quiz	Memory Recall based Quizzes	12 session		
Topics: Task and Task scheduler, Task States Context switching, scheduling algorithms, rate monotonic analysis, task management function calls, Concepts, scheduling, IPC, RPC, CPU Scheduling, scheduling criteria, scheduling algorithms Threads: Multi-threading models, synchronization Mutex: creating, deleting, prioritizing mutex, mutex internals, Messages, Buffers, mailboxes, queues, semaphores, deadlock, priority inversion						
Module 3	Process management	Assignment	Programming Assignment	12 session		
Topics:						

Resource sharing, Concept and function calls for:- Interrupt service routine, Semaphore, Message que, Event Registers, Pipes, Signals, Timers, Memory management, Communication Interfaces, Process stack management, run-time buffer size, swapping, overlays, block/page management, replacement algorithms, real-time garbage collection

Module 4	Real Time Operating Systems	Assignment	Programming Assignment	10 session

Topics:

Overview of various systems: - Linux POSIX system, RTLinux / RTAI, Windows system, MicroC/OS-II, VX Works, Free RTOS, Differences in operating systems.

List of Laboratory Tasks: Nil

Targeted Application & Tools that can be used:

Targeted Applications: Automotive, Healthcare, defense applications

Professionally Used Software: Embedded C, Linux/ Unix

Project Work/Assignment:

1. Case Study: At the end of the course students will be given a 'real-world' application-based on RTOS as a case study. Students will be submitting a report in appropriate format

2 Article review: At the end of the course a literature review of any 05 recent articles from the reputed national and international journal/ conferences will be given by students. They need to refer to tools like Scopus/ Google-Scholar and submit a report on their understanding of the assigned article in appropriate format.

3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to present their review work.

Text Book(s):

1. K. V. K. K. Prasad, "Embedded Real-Time Systems: Concepts, Design & Programming", Dream Tech Press, 2010, 3rd Edition
2. Sriram V Iyer, Pankaj Gupta, "Embedded Real Time Systems Programming", Tata Mc-Graw Hill, 2004. 2nd Edition

Reference(s):

Reference Book(s):

1. David. E. Simon, "An Embedded Software Primer", Addison- Wesley Professional, 1st Edition.
2. Raymond J.A. Buhr, Donald L. Bailey, "An Introduction to Real-Time Systems- From Design to Networking with C/C++", Prentice Hall, 1st Edition.
3. C.M. Krishna, Kang G. Shin, "Real-Time Systems", International Editions, Mc-Graw Hill, 1st Edition

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL online course:- https://nptel.ac.in/courses/106105036
2. University of Michigan : http://www.eecs.umich.edu/courses/eecs571/lectures/lecture1-intro.pdf
3. US-Texas online video content:- http://users.ece.utexas.edu/~gerstl/ee445m_s19/lectures.html
4. Online ppts:- https://www.cse.iitb.ac.in/~krithi/courses/684/ts-Sep-2004.pdf

5. https://presiuniv.knimbus.com/user#/home

E-content:

1. Yanbing Li, M. Potkonjak, W. Wolf, " Real-time operating systems for embedded computing", IEEE International Conference on Computer Design: VLSI in Computers and Processors, (ICCD), 12-15 Oct. 1997 https://ieeexplore.ieee.org/document/628899
2. Alireza Ejlali, Bashir M. Al-Hashimi, Petru Eles," Low-Energy Standby-Sparing for Hard Real-Time Systems", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, VOL. 31, issue.1 https://ieeexplore.ieee.org/document/6152774
3. Mastura D. Marieska, Paul G. Hariyanto, M. Firda Fauzan, Achmad Imam Kistijantoro, "On performance of kernel based and embedded Real-Time Operating System: Benchmarking and analysis", International Conference on Advanced Computer Science and Information System (ICACSIS), 17-18 Dec. 2011 https://ieeexplore.ieee.org/document/6140739
4. Takako Nonaka, Masato Shimano, Yuta Uesugi, Tomohiro Hase, "Structural Health Monitoring Framework Based on Internet of Things: A Survey", 10th International Conference on Intelligent Systems Design and Applications, 2010. https://ieeexplore.ieee.org/document/5687096

Topics relevant to "EMPLOYABILITY SKILLS":", MicroC/OS-II, VX Works, RTLinux, Free RTOS for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Mr. Kiran Dhanaji Kale
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18, Dated 03/08/2022

a. DISCIPLINE ELECTIVES

<table>
<tr><td>Course Code:

ECE5008</td><td colspan="3">Course Title: Software for Embedded System

Type of Course: Theory only</td><td>L-T-P-C</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>Version No.</td><td colspan="8">2.0</td></tr>
<tr><td>Course Pre-requisites</td><td colspan="8">Before attempting this course the student should have prior knowledge of Digital Logic and Operators, some understanding of Microprocessors and/or Microcontrollers, Assembly Language Programming of any Microprocessors and/or Microcontrollers, Prior C Programming knowledge (would be an added advantage but not compulsory).</td></tr>
<tr><td>Anti-requisites</td><td colspan="8">NIL</td></tr>
<tr><td>Course Description</td><td colspan="8">This course focuses on the development of software for real-world embedded systems. Students will be exposed to various techniques for writing efficient codes for embedded products.

The course will begin by giving an overview of controlling hardware systems using C programming language. In the next level use of Integrated Development Environment (IDE) tools will be undertaken for building and managing efficient programs and design. Installation of software tools as well as virtual machines, controlling of hardware kits etc. will be the key elements. To augment the learning process for independent software development students will be trained in compilation and make process by using various open-source compilers and tools such as GNU toolchain GNU, Git version control, Linux, Virtual Machines etc. Additionally, concepts like memory management, device driver development, compilers and debuggers, timers and interrupt systems, interfacing of devices, communications and networking in embedded systems will make students ready for industry.</td></tr>
<tr><td>Course Objective</td><td colspan="8">The objective of the course is to familiarize the learners with the software for embedded systems and attain SKILL DEVELOPMENT through PARTICPATIVE LEARNING</td></tr>
<tr><td>Course Outcomes</td><td colspan="8">On successful completion of this course the students shall be able to:

1. Summarize the concepts to develop software for real time embedded systems.
2. Write efficient programs with IDE tools for embedded systems.
3. Demonstrate various programming steps using open-source compilers and tools for embedded software development.
4. Explain various concepts of memory management, device drivers, timers and interrupt systems, interfacing of devices, communications and networking in embedded systems.</td></tr>
<tr><td>Course Content:</td><td colspan="8"></td></tr>
<tr><td>Module 1</td><td colspan="2">Introduction to Embedded Systems Software Development</td><td>Quiz</td><td colspan="2">Memory Recall based Quizzes</td><td colspan="2">7 session</td></tr>
<tr><td colspan="9">Topics:</td></tr>
</table>

Review of Embedded Systems and Application Areas, Fundamentals of Software Engineering and Development Processes, Embedded Software - Safety, Security and Quality, Introduction to Embedded Software Modelling, Context Diagrams, State Charts / Finite State Machines (FSMs),.				
Module 2	C-Programming for Embedded Systems	Assignment / Quiz	Programming	8 session
Topics: Review of modeling languages for Embedded Software development, C-Programming Review, Programming ARM Controllers using C – Conditional Statements, Loop Statements, debugging, single stepping, breakpoints, pointers and data structures, variables, numbers and parameter passing.				
Module 3	Memory Management and Device Driver Concepts	Assignment	Analysis and Verification	17 session
Topics: Introduction to Memory Organization, Memory Architectures, Memory Segments, Data Memory, Special Keywords (Const, Extern & Static), The Stack, The Heap, Code Memory, Practice on Memory Manipulation Software, Incorporate Memory Manipulation Software into the build system and Evaluation of some Test Functions. Linux - Scripting and Configuration, Kernel Building, Building Libraries and Utilities, Generic Device Driver Development Concepts, Linux Device Drivers.				
Project Work/Assignment:				
1.Case Studies: At the end of the course students will be given 'real-world' application-based circuits like traffic light controller, LCD display, DC motor etc. as a case study. Students will be submitting a report which will include Circuit Diagrams, Design, Working Mechanism and Results etc. in appropriate format. 2. Book/Article review: At the end of each module a book reference or an article topic will be given to an individual or a group of students. They need to refer to the library resources and write a report on their understanding about the assigned article in an appropriate format. Presidency University Library Link . 3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same. 4. Project Assignment: Assignment 1: Recently there have been lot of controversies over use of Electronic Voting Machine (EVM) Systems in elections. You have been asked to design an "EVM System" to be used in elections. The system will have additional facility to webcast the voting process live to a central station using Wi-Fi/3G/4G connection by using a high-resolution camera and/or tablet (as of now avoid VVPAT facility). Draw a FSM diagram considering various states, inputs and Outputs. Assignment 2:				

Consider the figure shown below showing the layout of an Embedded System to be designed using the TM4C123x/129x microcontroller. Write a device driver for the individual modules shown such as for stepper motor control, dc motor control, timer and sensing inputs both digital as well as analog.

Text Book(s):

1. Joseph Yiu, "*The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors*," 3rd Edition, Newnes.

Reference(s):

Reference Book(s):

1. Michael Barr and Anthony Massa, "*Programming Embedded Systems with C and GNU Development Tools*," O'Reilly.
2. Haring D.D. et al., "Embedded Software Development With C," Springer.
3. Jane W S Liu, "Real – Time Systems", Prentice Hall, 2000.
4. Class Notes (CN).

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Video lectures on "Embedded System using Arm" by Prof. Dr.Indranil Sen Gupta, IIT KGP Lecture 01: Introduction to Embedded Systems - YouTube
2. Lecture series on Embedded Systems by Dr.Santanu Chaudhury,Dept. of Electrical Engineering, IIT Delhi . For more details on NPTEL visit http://nptel.ac.in

E-content:

1. Camposano, R., & Wilberg, J. (1996). Embedded system design. *Design Automation for Embedded Systems*, *1*(1), 5-50. Embedded system design | SpringerLink
2. Ryu, S., & Kim, S. C. (2020). Embedded identification of surface based on multirate sensor fusion with deep neural network. *IEEE embedded systems letters*, *13*(2), 49-52. Embedded Identification of Surface Based on Multirate Sensor Fusion With Deep Neural Network | IEEE Journals & Magazine | IEEE Xplore

Topics relevant to "SKILL DEVELOPMENT": Introduction to Embedded Systems, C-Programming for Embedded Systems. Memory management concepts for C programming for Skill Development through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Mrs. Aruna Dore
Recommended by the Board of Studies on	15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Meeting No. 18th , Dated 03/08/2022

<table>
<tr><td>Course Code:
ECE5009</td><td colspan="4">Course Title: : ASIC Design and Modelling
Type of Course: Theory only</td><td>L-T-P-C</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>Version No.</td><td colspan="9">2.0</td></tr>
<tr><td>Course Pre-requisites</td><td colspan="9">Basic concepts of MOSFETs, Digital Design, Embedded Systems and Interfacing, Hardware Description Language</td></tr>
<tr><td>Anti-requisites</td><td colspan="9">NIL</td></tr>
<tr><td>Course Description</td><td colspan="9">This course aims to provide a strong foundation to understand the design of Application Specific Integrated Circuits (ASICs) design for real time digital systems. This course insight into the implementation Strategies for Digital ICs: Custom IC design, Cell-based design methodology. Array based implementation approaches critical physical design issues for future computing systems, and System-On-Chip (SOC) designs. Also, the course analyzes the timing issues in combinational and sequential logic design to represent the physical IC design procedures namely Partitioning, Floor Planning, Placement and Routing with its types.</td></tr>
<tr><td>Course Objective</td><td colspan="9">The objective of the course is to familiarize the learners with the concepts of ASIC Design and Modelling and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.</td></tr>
<tr><td>Course Outcomes</td><td colspan="9">On successful completion of this course the students shall be able to:
1. Demonstrate the characteristic of ASICs with Programming technologies of Logic Devices
2. Summarize the physical design process utilized in the design of ASICs
3. Analyze the faults and timing issues in the developed ASIC design
4. Classify the FPGA devices based on the architecture and design technology</td></tr>
<tr><td>Course Content:</td><td colspan="9"></td></tr>
<tr><td>Module 1</td><td colspan="3">Overview of ASIC and PLD</td><td>Quiz</td><td colspan="2">Memory Recall-based Quizzes</td><td colspan="2">10 sessions</td></tr>
<tr><td colspan="10">Topics:
Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs</td></tr>
<tr><td>Module 2</td><td colspan="3">ASIC Physical Design</td><td>Assignment / Quiz</td><td colspan="2">Memory Recall-based Quizzes</td><td colspan="2">10 sessions</td></tr>
<tr><td colspan="10">Topics:
System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction – DRC.</td></tr>
<tr><td>Module 3</td><td colspan="3">Logic Synthesis, Simulation and Testing</td><td>Assignment</td><td colspan="2">Analysis and Verification</td><td colspan="2">10 sessions</td></tr>
</table>

Topics:

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

Module 4	FPGA Testing	Assignment	Memory Recall-based Quizzes	10 sessions

Topics:

Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology - mapping for FPGAs ,FPGA Verification Techniques, PLB Architecture, BIST Architecture using Diagnostic Procedure Xilinx XC4000 - ALTERA's FLEX 8000/10000, and their speed performance

Project Work/Assignment:

1. Case Studies: At the end of the course students will be given case studies on Xilinx XC4000 and ALTERA's FLEX 8000 in the appropriate format.

2. Book/Article review: At the end of each module a book reference or an article topic will be given to an individual or a group of students. They need to refer to the library resources and write a report on their understanding of the assigned article in the appropriate format. Presidency University Library Link .

3. Presentation: There will be a seminar presentation, where the students will be given a topic. They will have to explain/teach the working and discuss the applications for the same.

4. Project Assignment: (Don't be specific)

Reconfigured VLSI architecture for DSRC applications. This topic mainly gives information on how ITS concepts can be used to provide more safety and leisure in traveling at a low cost.

DSRC (Dedicated short-range communication) is wireless communication technology. It enables different users to be better informed, and make safer, more coordinated, and advanced use of transportation networks. ITS has provided this unique service. DSRC can be classified into two categories. These are automobile to automobile and automobile to roadside.

DSRC uses FM0 and Manchester codes for encoding. The diversity between the 2 codes limits the potential to design fully reused VLSI architecture for both codes. SOLS is used to design fully reused VLSI architecture.

In this VLSI design project, with this the Similarity oriented logic simplification techniques (SOLS) technique and many more techniques discussed above result in improvement in HUR, area optimization, reduced power consumption, lower latency, and elimination of many other limitations on hardware utilization.

The FM0 and Manchester encoders are designed with these techniques to achieve high speed and fully reconfigured VLSI architecture for the application system.

Assignment 1: Implement Programmable Logic Devices: ROMs and EPROMs – PLA –PAL using Cadence tool

Assignment 2: Case studies

1. M.J.S .Smith, "*Application Specific Integrated Circuits*", 1st Edition, Addison – Wesley Longman Inc., 1997.
2. Naveed Sherwani, "*Algorithms for VLSI Physical design automation*", 3rd Edition, Springer International edition, 2005.

Reference(s):

Reference Book(s):

1. Himanshu Bhatnagar, "*Advanced ASIC Chip Synthesis*",2nd Edition, Kluwer Academic Publisher, 2002
2. Farzad Nekoogar, "*Timing Verification of Application-Specific Integrated Circuits*", 1st Edition, Farzad Nekoogar, Prentice-Hall. 1999.
3. J. Bhaskar, "Verilog HDL for synthesis",1st Edition, BS Publication,2004:

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL Course on VLSI Design Verification and test, by Dr. Santosh Biswas, Prof.Jatindra Kumar Deka, Prof.Arnab sarkar, IIT Guwahati. https://nptel.ac.in/courses/117103125

2. NPTEL Course on VLSI Circuits, by Prof. S. Srinivasan, IIT Madras. https://nptel.ac.in/courses/117106092

E-content:

1. C.-Y. Lee; F.V.M. Catthoor; H.J. de Man, "An efficient ASIC architecture for real-time edge detection", IEEE Transactions on Circuits and Systems, Volume: 36, Issue: 10, October 1989, pp: 1350-1359. https://ieeexplore.ieee.org/document/44350
2. Masudul Hassan Quraishi , Erfan Bank Tavakoli, and Fengbo Ren, "A Survey of System Architectures and Techniques for FPGA Virtualization", IEEE Transactions on Parallel and Distributed Systems, Vol. 32, No. 9, September 20, pp: 2216-2230. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9369140
3. MJ, S. P. Comprehensive Study of Popular VLSI Test Scan Architecture. https://www.ijert.org/comprehensive-study-of-popular-vlsi-test-scan-architecture

Topics relevant to "EMPLOYABILITY SKILLS": ASIC Design and Floor planning," FPGA architecture and FPGA fabrics, FPGA testing for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Mrs. Aruna Dore
Recommended by the Board of Studies on	15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Meeting No. 18th , Dated 03/08/2022

<table>
<tr><td>Course Code:
ECE5010</td><td colspan="3">Course Title: Design for Testability
Type of Course: Theory only</td><td>L- T-P- C</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>Version No.</td><td colspan="8">2.0</td></tr>
<tr><td>Course Pre-requisites</td><td colspan="8">Basic concepts of Digital Logic Circuits using gates, flip-flops, registers, multiplexers, decoders etc. Basic electronic Circuits and Mathematics and Fundamentals of VLSI Design-based systems.</td></tr>
<tr><td>Anti-requisites</td><td colspan="8">NIL</td></tr>
<tr><td>Course Description</td><td colspan="8">This course provides an in-depth theory of fault analysis, test generation, and design for testability for digital VLSI circuits and systems. Design and manufacturing defect models are introduced along with test generation and fault simulation algorithms targeting the different fault models. Both combinational and sequential logic testing are covered, and different synthesis for testability schemes such as BIST (Built-In-Self-Test), scan path design, and Core based testing are introduced. The course also demonstrates the test compression and compaction schemes such as code-based schemes, linear decompression based schemes and test response compaction.</td></tr>
<tr><td>Course Objective</td><td colspan="8">The objective of the course is to familiarize the learners with the concepts of design for testability and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.</td></tr>
<tr><td>Course Outcomes</td><td colspan="8">On successful completion of this course the students shall be able to:
1. Interpret the concepts of testing which can help to design a better yield in IC design.
2. Discuss the generation of test patterns.
3. Analyze the various test generation methods
4. Summarize the BIST techniques for improving testability.</td></tr>
<tr><td>Course Content:</td><td colspan="8"></td></tr>
<tr><td>Module 1</td><td colspan="2">Introduction to DFT and Fundamentals of DFT</td><td colspan="2">Assignment/Quizzes</td><td colspan="2">Memory Recall based Quizzes</td><td colspan="2">10 Sessions</td></tr>
<tr><td colspan="9">Topics:
Fundamentals of fault analysis, test generation, and design for testability for digital VLSI circuits and systems, Exhaustive Testing and basics of testing, ASIC Flow, DFT Basics, Chip Fabrication Process, ATE Basics.</td></tr>
<tr><td>Module 2</td><td colspan="2">Scan Insertion and compression</td><td colspan="2">Assignment</td><td colspan="2">Simulation and analysis task</td><td colspan="2">10 Sessions</td></tr>
<tr><td colspan="9">Topics:
Scan Design Basics, Scan Golden Rules, Scan DRC Checks, Scan Insertion, Generate test protocol and understanding, Lock-Up Latches, Basics for Compression, Compression Techniques, On-Chip-Clocking, hierarchical and boundary scan. Controllability and Observability and related issues.</td></tr>
<tr><td>Module 3</td><td colspan="2">Introduction to ATPG</td><td colspan="2">Assignment/Quizzes</td><td colspan="2">Design Analysis</td><td colspan="2">10 Sessions</td></tr>
</table>

Topics:

Fault models, Fault classes, Pattern generation and simulation, simulations and debugging, Diagnosis flow and fault simulation. Automatic Test Pattern Generation (ATPG) in DFT, ATPG classification, Combinational ATPG (e.g. D, PODEM, FAN), Sequential ATPG.

Module 4	BIST Architecture, Memory BIST, Logic BIST	Assignment/Project	Data Analysis	10 Sessions

BIST Design Rules, Test Pattern Generation ,Exhaustive Testing ,Pseudo-Random Testing, ,Delay Fault Testing, BIST Architectures circuits with scan chain.

Targeted Application & Tools that can be used:

Application Area – Hardware design Engineer, DFT engineer, VLSI design Engineer.

Professionally Used Software: Cadence-Modus, Tessent

Project work/Assignment:

1. Article review: At the end of course an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link .

2. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

3. Project Assignment:-

Project 1. The emphasis on online education is increasing now-a-days, based on the current scenario, one organization designs a prototype for smooth and interactive learning platforms, consider the design with following functions embedded:

1.Locking of meeting after 10 minutes

2.Control over the class by the instructor

You are free to add functions. Enlist the test cases and pattern you will use to test the design.

Assignment 1. A block level design is given as a project to design engineer, it is given for DFT engineer for testing, he/she needs to insert scan and generate patterns, to get the required test coverage. What will be your approach for the same?

Assignment 2. ALU is the heart of the processors, The basics ones start with 4 bit and beyond. Analyze the test patterns for 4 bit ALU in HDL environment and use test patterns for testing the design.

Textbook(s):

1. Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, "*VLSI Test Principles and Architectures*" The

Morgan Kaufmann, 2013

References:

Reference Book(s):

Z.Navabi, "*Digital System Test and Testable Design*", Springer, 2011.

2. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, System-on-Chip Test Architectures: Nanometer Design for Testability, Morgan Kaufmann, First Edition, 2010.
3. Huertas JL, (editor), "Test and design-for-testability in mixed-signal integrated circuits", The Netherlands: Kluwer Academic; 2004.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Lecture videos for design for testability: https://onlinecourses.nptel.ac.in/noc20_ee76
2. PPT on Design for Testability, Link : https://eecs.ceas.uc.edu/~jonewb/DFTnew.pdf
3. https://www.youtube.com/watch?v=MgCFUO2BrkQ
4. https://www.youtube.com/watch?v=MEaMm423t0w&list=PLZjlBaHNchvOFBWBAtAP9exwQgYpKqsO4
5. https://www.geeksforgeeks.org/design-for-testability-dft-in-software-testing/
6. https://web.stanford.edu/class/archive/ee/ee371/ee371.1066/lectures/lect_14.2up.pdf

E-Content

1. Bukovjan, Peter, Meryem Marzouki, and Walid Maroufi. "Design for testability reuse in synthesis for testability." *Proceedings. XII Symposium on Integrated Circuits and Systems Design (Cat. No. PR00387)*. IEEE, 1999.

2. Williams, Thomas W. "Design for Testability: The Path to Deep Submicron." *14th Asian Test Symposium (ATS'05)*. IEEE, 2005.

3. Williams, Thomas W. "Design for testability: today and in the future." *VLSI Design, International Conference on*. IEEE Computer Society, 1997.

4. Williams, Thomas W., and Kenneth P. Parker. "Design for testability—A survey." *Proceedings of the IEEE* 71.1 (1983): 98-112.

5.Ghosh, Indradeep, Niraj K. Jha, and Sujit Dey. "A low overhead design for testability and test generation technique for core-based systems-on-a-chip." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 18.11 (1999): 1661-1676.

Topics relevant to "EMPLOYABILITY SKILLS": Fault models, Fault classes, Pattern generation and simulation, simulations and debugging, Diagnosis flow and fault simulation ATPG, BIST, Projects based on Various design for testability recently published research articles for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Ms Akshaya M Ganorkar
Recommended by the Board of Studies on	15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Meeting No. 18th , Dated 03/08/2022

<table>
<tr><td>Course Code:
ECE5011</td><td colspan="3">Course Title: CAD for VLSI
Type of Course: Theory only</td><td>L-T-P-C</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>Version No.</td><td colspan="8">2.0</td></tr>
<tr><td>Course Pre-requisites</td><td colspan="8">Basic concepts of Digital Electronics, VLSI design flow, VLSI circuits implementation for complex digital and analog systems.</td></tr>
<tr><td>Anti-requisites</td><td colspan="8">NIL</td></tr>
<tr><td>Course Description</td><td colspan="8">The purpose of this course is to introduce the fundamentals techniques and algorithms used in Computer-Aided Design. This course insight into the modelling, analysis, computer-aided design (CAD) algorithms for real time VLSI applications. The course develops design skills to apply algorithms related to physical design of VLSI circuits.</td></tr>
<tr><td>Course Objective</td><td colspan="8">The objective of the course is to familiarize the learners with the concepts of CAD tools and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.</td></tr>
<tr><td>Course Outcomes</td><td colspan="8">On successful completion of this course the students shall be able to:
1. Demonstrate the graph theory algorithms utilized in VLSI Design.
2. Apply the algorithms of Partitioning, Placement and Floor planning in the VLSI IC design.
3. Analyse the computational complexity of physical design algorithms.
4. Illustrate the routing algorithms and its employment in the IC fabrication.</td></tr>
<tr><td>Course Content:</td><td colspan="8"></td></tr>
<tr><td>Module 1</td><td colspan="2">Design methodologies and CAD tools</td><td>Quiz</td><td colspan="2">Memory Recall based Quizzes</td><td colspan="2">10 classes</td></tr>
<tr><td colspan="9">Topics:
Design domains, design actions, design methods and technologies, VLSI Design automation tools, data structure for graph representation, Graph algorithms: depth first search, breadth first search, Dijkstra’s algorithm and prim’s algorithm.</td></tr>
<tr><td>Module 2</td><td colspan="2">Computational complexity and layout compaction</td><td>Assignment</td><td colspan="2">Design Analysis</td><td colspan="2">9 classes</td></tr>
<tr><td colspan="9">Topics:
Combinatorial optimization problems, decision problems, Complexity classes, NP completeness and NP hardness, symbolic layout, applications of compaction, informal problem formulation, maximum distance constraints, and algorithms for constraint graph compaction.</td></tr>
<tr><td>Module 3</td><td colspan="2">Placement, Partitioning and Floor planning</td><td>Assignment</td><td colspan="2">Design Analysis</td><td colspan="2">10 classes</td></tr>
</table>

Topics:

Wire length estimation, Types of placement problem, placement algorithms-constructive placement, iterative improvement, KL partitioning algorithm, floor planning concepts-terminology, representation and problems, shape functions and floor plan sizing.

Module 4	Routing and Logic Synthesis	Assignment	Programming and simulation	9 classes

Topics:

Area routing, channel routing-models, vertical and horizontal constraint graphs, left edge algorithm, channel routing algorithms, introduction to combinational logic synthesis, Binary decision diagrams: ROBDD principles, implementation, construction and manipulation and two level logic synthesis.

List of Laboratory Tasks: Nil

Targeted Application & Tools that can be used:

Targeted Applications: Application Areas are aspects of Computational Circuit Analysis, VLSI Circuit Analysis, Timing Verification and Optimization, Design and Layout Generation.

Professionally Used Software: VHDL compiler and simulator, logic synthesis tools, and automatic place and route tools available with Vivado design suit.

Project work/Assignment:

Book/Article review: At the end of each module a book reference or an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link .

Presentation: There will be a group presentation on the topics Breadth-first search, Algorithms for Constraint-graph Compaction, Placement Algorithms Assignment, Routing Algorithms, where the students have to explain/demonstrate the working and discuss the applications for the same.

Assignment:

1. Develop a heuristic algorithm for finding a maximum bipartite subgraph in circle graphs.
2. Suggest modifications to the Kernighan-Lin algorithm to speed up the algorithm.
3. Design an efficient heuristic algorithm based on maze routing to simultaneously route two 2-terminal nets on a grid graph. Compare the routing produced by this algorithm with that produced by Lee's maze router by routing one net at a time.
4. Implement the approximation algorithm for finding a *k*-independent set in circle graphs.
5. Experimentally evaluate the performance of the algorithm by implementing an exponential time complexity algorithm for finding a *k*-independent set.

Text Book(s):

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2006 2nd Edition.
2. M. L. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI circuits", 2001 2nd Edition.

Reference(s):

1. Stephen Trimberger, "Introduction to CAD for VLSI", Kluwer Academic publisher, 2002.
2. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, 2nd edition.
3. G. Hachtel and F. Somenzi, "Logic Synthesis and Verification Algorithms", Kluwer, 1998.
3. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers; 3rd ed., 1999.

Online and Web resource (s):

1. Lecture videos for CAD for VLSI Design Part 1 by Prof. V. Kamakoti and Shankar Balachandran Department of Computer Science Engineering, IIT Madras - https://nptel.ac.in/courses/106/106/106106088/
2. Power point slides for CAD for VLSI by IIT Kharagpur - http://www.facweb.iitkgp.ac.in/~isg/CAD/
3. Lecture video on important CAD tools by Prof. Hitesh Dholakiya by Engineering Funda - https://www.youtube.com/watch?v=hJTK5nj1iq8
4. Lecture video on important VLSI CAD Part-1 by Prof. Rob. A. Rutenbar by University of Illinois - https://www.youtube.com/watch?v=WLdbujc-aH4
5. Lecture video on important VLSI CAD Part-2 by Prof. Rob. A. Rutenbar by University of Illinois - https://www.youtube.com/watch?v=zkFRfmySFOw

Presidency University Library Link:

https://presiuniv.knimbus.com/user#/home

E-Content:

1. Cong, J. Kahng, A.B. Kwok-Shing Leung " Efficient algorithms for the minimum shortest path Steiner arborescence problem with applications to VLSI physical design" in IEEE transactions on computer Aided Design of Circuits and Systems, Volume: 17, Issue: 1, January 1998, doi:10.1109/43.673630, https://puniversity.informaticsglobal.com:2069/document/673630
2. Dewan, Monzurul Islam; Kim, Dae Hyun "NP-Separate: A New VLSI Design Methodology for Area, Power, and Performance Optimization" in IEEE transactions on computer Aided Design of Circuits andSystems,doi:10.1109/TCAD.2020.2966551. https://puniversity.informaticsglobal.com:2069/document/8957675
3. H. Martin Bucker and Christian Sohr Bucker "Reformulating a Breadth-First Search Algorithm on an Undirected Graph in the Language of Linear Algebra" in IEEE 2014 International Conference on Mathematics and Computers in Sciences and in Industry, 33–35. doi:10.1109/MCSI.2014.40
https://ieeexplore.ieee.org/abstract/document/7046157
4. Farnaz Towhidi, Arash Habibi Lashkari "Binary Decision Diagram (BDD)" in IEEE 2009 International conference on future computer and communication, 03-05 April 2009, doi:10.1109/ICFCC.2009.31 https://ieeexplore.ieee.org/abstract/document/5189833.

Topics relevant to "EMPLOYABILITY SKILLS": Design Methodologies, Algorithmic Graph Theory, Tractable and Intractable Problems, Layout compaction, Placement and Partitioning, floor planning, Routing for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Ms. R Anusha
Recommended by the Board of Studies on	15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Meeting No. 18th , Dated 03/08/2022

Course Code: ECE5012	Course Title: Reconfigurable Computing Type of Course: Theory only	L-T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Basic concepts of Microprocessor & Micro-Controller, CPLD, FPGA and their architectures. Basics of high level programming concepts and Hardware Description Language with synthesis.					
Anti-requisites	NIL					
Course Description	In recent times, the VLSI technology has triggered a novel architecture for computers that utilizes the parallelism concept in real time applications. The advent of reconfigurable computing provided versatility in the hardware circuitry, with high accuracy in computing and overcoming the fixed hardware configurations as present in conventional digital controllers. In this course, the students will comprehend the advanced reprogramming computation used in hardware and software. This course will enhance the basic of configurability in real time application. The purpose of the course reconfigurable computing is to instruct students about the possibilities and rapidly growing interest in adaptive hardware and corresponding design techniques by providing them the necessary knowledge for understanding and designing reconfigurable hardware systems and studying applications benefiting from dynamic hardware reconfiguration.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of reconfigurable computing and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: CO1 - Illustrate partial reconfiguration for various applications using peripheral devices. CO2 - Develop the reconfigurable system using HDL and FPGAs. CO3 - Demonstrate an embedded system on FPGA using IP blocks. CO4 - Analyze the reconfigurable computing in various applications for block optimization in FPGA.					
Course Content:						
Module 1	Reconfigurable Computing	Quiz	Comprehension	11 session		
Topics: Reconfigurable Computing Systems, Evolution and Characteristics, Advantages and Issues, Fundamental Concepts and Design Steps, Domain Specific Processors and Application Specific Processors.						
Module 2	Reconfigurable Architectures	Assignment / Case Study	Application	12 session		

Topics: Classification of Reconfigurable Architectures, FPGA Technology and Architectures, LUT devices and Mapping, Placement and Partitioning. Interconnections in Reconfigurable Architectures: Routing and Switching concepts.				
Module 3	Programming Technology	Assignment	Analysis	10 session
Topics: HDL Based Programming and High level Synthesis using C, Partial Reconfiguration.				
Module 4	Intellectual Property Based Design	Project	Application	9 session
Topics: Intellectual Property Based Design: Soft core, Firm core and Hard Core, Software tools.				

Project Work/Assignment:

1. Case Studies: At the end of the course students will be given case study on "IP based design in VLSI". Students will be submitting a report in appropriate format.

2. Presentation: Individual presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

3. Project Assignment: The project work will be given on "Configurability in FPGA based Digital Design" and the students have to complete the work using the Cadence tools and documentation of the entire work in prescribed format to be submitted.

Assignment 1: Different Placement and Routing algorithms in FPGA

Assignment 2: Validation of Advanced Digital Design using the Xilinx Vivado Tool

Text Book(s):

1. S. Hauck ,"Reconfigurable Computing: Theory and practice of FPGA based Computation", 2nd Edition, Morgan Kaufmann, 2008.
2. Simon, "Programming FPGA's: Getting started with Verilog",1st Edition, Mc Graw – Hill Education,2016.
3. Wayne Wolf, "FPGA-Based System Design",1st Edition, Pearson Education, , 2005.

S. Palnitkar,"Verilog HDL",Pearson Education, 1st Edition, 2003.

Reference(s):

Reference Book(s):

1. M. Gokhale and P. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", 2nd Edition, Springer, 2005.
2. C. Maxfield, "The Design Warrior's Guide to FPGAs", 1st Edition, Newnes, 2004.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL Course on "Digital System design with PLDs and FPGAs" by Prof. Kuruvilla Varghese https://www.digimat.in/nptel/courses/video/117108040/L01.html
2. NPTEL COURSE on "FPGA Architecture and Programming using Verilog HDL" by Dr. Jayaraj U Kidav, https://elearn.nptel.ac.in/shop/partnering-courses/lab-workshop-fpga-architecture-and-programming-using-verilog-hdl/

E-content:

1. Sara M. Mohamed , Wafaa S. Sayed , Ahmed G. Radwan, and Lobna A. Said, "FPGA Implementation of Reconfigurable CORDIC Algorithm and a Memristive Chaotic System With Transcendental Nonlinearities", IEEE Transactions on Circuits And Systems—I: Regular Papers, April 2022, pp:1-8. https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9759515
2. Jixuan Li, Ka-Fai Un , Member, IEEE, Wei-Han Yu , Member, IEEE, Pui-In Mak,

<table>
<tr><td>Fellow, IEEE, and Rui P. Martins, "An FPGA-Based Energy-Efficient Reconfigurable Convolutional Neural Network Accelerator for Object Recognition Applications", IEEE Transactions on Circuits and Systems—II: Express Briefs, Vol. 68, No. 9, September 2021, pp: 3143-3147. https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9476039
3. Rui Yao, Yinhua Zhao , Yongchuan Yu, Yihe Zhao, and Xueyan Zhong, "Fast Search and Efficient Placement Algorithm for Reconfigurable Tasks on Modern Heterogeneous FPGAs", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 30, No. 4, April 2022, pp: 474-487. https://ieeexplore.ieee.org/document/9728733/authors#authors
Joao MP Cardoso, Andre DeHon, and Laura Pozzi, "Guest Editorial: IEEE TC Special Section on Compiler Optimizations for FPGA-Based Systems", IEEE Transactions on Computers, Vol. 70, No. 12, December 2021, pp: 2013-2014. https://ieeexplore.ieee.org/document/9605656</td></tr>
<tr><td>Topics relevant to "EMPLOYABILITY SKILLS": Domain Specific Processors and Application Specific Processors, Reconfigurable Architectures, FPGA Technology and Architectures, Intellectual Property Based Design for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.</td></tr>
</table>

Catalogue prepared by	Dr. Joseph Anthony Prathap
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE5013	Course Title: VLSI Architecture Type of Course: Theory only		L-T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Basic concepts of VLSI Design, FPGA, memory devices, and digital integrated circuits					
Anti-requisites	NIL					
Course Description	This course provides insights into the fundamentals of FPGA architecture, FPGA fabrics. The course develops the knowledge of both hardware and software that leads to the design and implementation of both analog and digital VLSI circuits. The course emphasizes FPGA fabric architecture, highlighting design implementation using FPGA and PLDs.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of reconfigurable computing and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: 1. understand the FPGA architectures 2. understand FPGA fabrics 3. understand combinational and sequential machines 4. develop logic implementation using FPGAs 5. develop logic implementation using PLDs					
Course Content:						
Module 1	FPGA FABRICS	Quiz	Memory Recall-based Quizzes	10 sessions		
Topics: Introduction, FPGA architectures, SRAM-based FPGAs, permanently programmed FPGAs, Chip input/output, Circuit design of FPGA fabrics, Architecture of FPGA fabrics.						
Module 2	COMBINATIONAL LOGIC AND SEQUENTIAL MACHINES	Assignment / Quiz	Memory Recall-based Quizzes	10 sessions		
Topics: Introduction, Logic design process, combinational network delay, power, and energy optimization, arithmetic logic, sequential machine design process, sequential design styles, rules for clocking, performance analysis.						
Module 3	LOGIC IMPLEMENTATION USING FPGAs	Assignment	Analysis and Verification	10 sessions		
Topics: Syntax-directed translation, logic implementation by macro, logic synthesis, technology-independent, and dependent logic optimizations, physical design for FPGAs, and logic design process revisited.						
Module 4	INTRODUCTION TO	Assignment	Memory	10		

	PLDS		Recall-based Quizzes	sessions

Topics:

Introduction to PLDs, programmable sum-of-products arrays, PAL fuse matrix and, combinational outputs, PAL outputs with programmable polarity, PAL devices with programmable polarity, universal PAL, and generic array logic.

Project Work/Assignment:

1. Case Studies: At the end of the course students will be given case studies on Xilinx XC4000 and ALTERA's FLEX 8000 in the appropriate format.

2. Book/Article review: At the end of each module a book reference or an article topic will be given to an individual or a group of students. They need to refer to the library resources and write a report on their understanding of the assigned article in the appropriate format. Presidency University Library Link .

3. Presentation: There will be a seminar presentation, where the students will be given a topic. They will have to explain/teach the working and discuss the applications for the same.

4. Project Assignment:

Reconfigured VLSI architecture for DSRC applications. This topic mainly gives information on how ITS concepts can be used to provide more safety and leisure in traveling at a low cost. DSRC (Dedicated short-range communication) is wireless communication technology. It enables different users to be better informed, and make safer, more coordinated, and advanced use of transportation networks. ITS has provided this unique service. DSRC can be classified into two categories. These are automobile to automobile and automobile to roadside. DSRC uses FM0 and Manchester codes for encoding. The diversity between the 2 codes limits the potential to design fully reused VLSI architecture for both codes. SOLS is used to design fully reused VLSI architecture. In this VLSI design project, with this the Similarity oriented logic simplification techniques (SOLS) technique and many more techniques discussed above result in improvement in HUR, area optimization, reduced power consumption, lower latency, and elimination of many other limitations on hardware utilization. The FM0 and Manchester encoders are designed with these techniques to achieve high speed and fully reconfigured VLSI architecture for the application system.

Assignment 1: Implement various digital circuits using FPGA

Assignment 2: VLSI architecture for delay efficient 32-bit multiplier.

Text Book(s):

1. Wayne Wolf (2004), FPGA Based System Design, Pearson Education, New Delhi.
2. Robert Dueck (2005), Digital design With CPLD Applications and VHDL, Thomson Learning, USA.

Reference(s):

Reference Book(s):

1. Vikram Arkalgud (2011), VLSI Design: A Practical Guide for FPGA and ASIC Implementations, Springer Science, USA.
2. Leo Chartrand (2003), Advanced Digital Systems: Experiments & Concepts with CPLD's, Thomson Learning, USA

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Video lectures on "Architectural Design of digital Integrated circuits" by Prof. Indranil Hatai, IIT KGP
   https://onlinecourses.nptel.ac.in/noc21_ee52/preview

2. PG Level Advanced Certification Programme in VLSI Chip Design
   https://iisc.talentsprint.com/vlsi/index.html

E-content:

1. Fan, Y. C., Yu, Q., Schumann, T., Chien, Y. R., & Lu, C. C. (2014). Advanced VLSI Architecture Design for Emerging Digital Systems. VLSI Design, 2014, 746132-1.
   https://www.hindawi.com/journals/vlsi/2014/746132/

2. Vasanth, K., Sindhu, E., & Varatharajan, R. (2019). VLSI architecture for Vasanth sorting to denoise image with minimum comparators. Microprocessors and Microsystems, 71, 102880.
   https://www.sciencedirect.com/science/article/pii/S0141933119302522

3. MJ, S. P. Comprehensive Study of Popular VLSI Test Scan Architecture.
   https://www.ijert.org/comprehensive-study-of-popular-vlsi-test-scan-architecture

4. Moses, C. J., Selvathi, D., & Sophia, V. M. (2014). VLSI Architectures for Image Interpolation: A Survey. VLSI Design.
   https://www.hindawi.com/journals/vlsi/2014/872501/

Topics relevant to "EMPLOYABILITY SKILLS": FPGA architecture and FPGA fabrics, Scaling and Design Rules, Performance analysis of sequential machines, FPGA and PLD for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. Manikandan M
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE5014	Course Title: Networked Embedded Applications Type of Course: Theory only		L- T-P- C	3	0	3
Version No.	2.0				
Course Pre-requisites	Computer Networks, Embedded Systems				
Anti-requisites	NIL				
Course Description	This course deals with the three main application areas of Network Embedded Systems – Wireless Sensor Networks, Automotive, and Industrial Automation and relatively new subtopic of Home Automation.				
Course Objective	The objective of the course is to familiarize the learners with the concepts of networked embedded applications and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.				
Course Outcomes	On successful completion of this course the students shall be able to: 1) Summarize the basics of wireless networks and understand the architectures more effectively 2) Classify the wired and wireless embedded systems 3) Apply the embedded networks for car domains 4) Differentiate the intra and inter-vehicular network embedded systems				
Course Content:					
Module 1	Wireless Sensor Networks	Quiz	Memory Recall based Quizzes	15 Session	
Topics: Introduction to Wireless Sensor Network Technologies and Applications, WSN Architectures, WSN Design Challenges, WSN Deployment, WSN Protocol Stack - Time Synchronization, Localization, MAC, Routing, Applications, Building & Debugging WSN.					
Module 2	Industrial Automation in Network Embedded Systems	Quiz	Real time Application Project	15 Sessions	
Topics: Computer Integrated Manufacturing & Field Buses, Wired and Wireless Ethernet based Network Embedded Systems, Industrial Networks - Modified Ethernet, Top of Ethernet, Top of TCP/IP. Wireless Industrial Networks, Hybrid Wired and Wireless Systems.					
Module 3	Vehicular Networked Embedded Systems	Assignment	Memory Recall based Quizzes	10 Sessions	
Embedded Networks for Car Domains, Intra vehicular Network Embedded Systems - Event Triggered Systems, Time Triggered Systems. Inter-Vehicular Network Embedded Systems.					
List of Laboratory Tasks: Nil					

Targeted Application & Tools that can be used:

Targeted Applications: Automotive Systems, Fitness Trackers, GPS Systems, Internet of Things, Surveillance and monitoring for security, Blind spot warning, etc.,

Professionally Used Software: Arduino, Raspberry Pi, Network Simulator

Project Work/Assignment:

1. Article review: At the end of course an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link .

2. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

3. Project Assignments:- Implementations of embedded system concepts in Arduino & Raspberry pi boards and wireless sensor networks using Network Simulator

Text Book(s):

1. R.Zurawski, "*Network Embedded Systems*", CRC press, 2009. 2nd Edition

Reference(s):

Reference Book(s):

1. G.Pottie, W.Kaiser, "*Principles of Embedded Networked System Design*", Cambridge University Press, 2005, 2nd Edition.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL online content: https://nptel.ac.in/courses/108102045
2. NPTEL online content: https://nptel.ac.in/courses/108105057
3. Online notes: https://www.tutorialspoint.com/what-are-wireless-sensor-networks

E-content:

1. Fummi, F., Quaglia, D., & Stefanni, F. (2008, September). A SystemC-based framework for modeling and simulation of networked embedded systems. In *2008 Forum on Specification, Verification and Design Languages* (pp. 49-54). IEEE. https://ieeexplore.ieee.org/abstract/document/4641420

2. Bello, L. L., Mariani, R., Mubeen, S., & Saponara, S. (2018). Recent advances and trends in on-board embedded and networked automotive systems. *IEEE Transactions on Industrial Informatics*, *15*(2), 1038-1051. https://ieeexplore.ieee.org/document/8521696

3. Sandberg, H., Amin, S., & Johansson, K. H. (2015). "*Cyberphysical security in networked control systems: An introduction to the issue*". *IEEE Control Systems Magazine*, *35*(1), 20-23. https://ieeexplore.ieee.org/document/7011179

Topics relevant to "EMPLOYABILITY SKILLS": Wireless Industrial Networks, Vehicular Network Embedded Systems, Ethical considerations while developing Vehicular Embedded network model. Computer Integrated Manufacturing & Field Buses, Wired and Wireless Ethernet based Network Embedded Systems for developing Employability Skills through

Participative Learning techniques. This is attained through assessment component mentioned in course handout.	
Catalogue prepared by	Dr. T. Prabhu
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE5015	Course Title: Network Security Type of Course: Theory only	L- T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Computer Networks and Protocols					
Anti-requisites	NIL					
Course Description	The course is a study of fundamental concepts and principles of computing and network security. The course covers basic security topics, including symmetric and public key cryptography, digital signatures, cryptographic hash functions, authentication pitfalls, and network security protocols. It covers the underlying principles and techniques for network and communication security. Practical examples of security problems and principles for countermeasures are given. The course also surveys cryptographic and other tools used to provide security and reviews how these tools are utilized in protocols and applications.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of network security and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: 1) Summarize the basics of network security and understand the modes of operation 2) Explain the concepts of various Encryption techniques 3) Analyze the major security issues associated with the system and network security techniques 4) Apply standard security tools					
Course Content:						
Module 1	Introduction	Quiz	Memory Recall based Quizzes	8 Sessions		
Topics: Introduction to Classical and Modern Techniques: Attacks, Services and Mechanisms, Classical Encryption Techniques, DES, Block Cipher, Design Principles and Modes of Operation.						
Module 2	Encryption Techniques	Assignment/ Quiz	Real time Application Project	8 Sessions		
Topics: Encryption Algorithms and Hash Functions: Triple DES, RC5, Key Management, Public Key Cryptography, RSA Algorithm, Digital Signatures and Authentication Protocols.						
Module 3	System Security & Network Security	Assignment/ Quiz	Memory Recall based Quizzes	15 Sessions		
System Security: Backups, integrity Management, Protecting against Programmed Threats,						

Viruses and

Worms, Physical Security, Personnel Security. Network Security: Protection against Eavesdropping, Security for Modems, IP Security, Web Security, Electronic Mail Security, Authentication, Applications.

Module 4	Security Tools	Assignment/ Quiz	Memory Recall based Quizzes	9 Sessions

Security Tools: Firewalls, Wrappers, Proxies, Discovering a Break-in, Denial of Service Attacks and

Solutions, Cryptographic Security Tools: KERBEROS, PGP, SSH, SRP, OPIE.

Targeted Application & Tools that can be used:

Targeted Applications: Network Security involves access control, virus and antivirus software, application security, network analytics, types of network-related security (endpoint, web, wireless), firewalls, VPN encryption and more

Professionally Used Software: Security Tools: Firewalls, Wrappers, Proxies, Discovering a Break-in, Denial of Service Attacks and Solutions. Cryptographic Security Tools: KERBEROS, PGP, SSH, SRP, OPIE.

Project Work/Assignment:

1. Article review: At the end of course an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link .

3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

4. Project Assignments: Implementation of various concepts in network security using Cryptographic security tools.

Text Book(s):

1. William Stallings, "*Cryptography and Network Security: Principles and Practice*", Pearson. Sixth Edition.

Reference(s):

Reference Book(s):

1. M. Speciner, R. Perlman, C. Kaufman, "*Network Security: Private Communications in a Public World*", Pearson. Second Edition.
2. Michael Gregg, "*The Network Security Test Lab: A Step-By-Step Guide*", Wiley. First Edition.
3. J. Michael Stewart, Denise Kinsey, "*Network Security, Firewalls, and VPNs*", Jones & Bartlett Learning. Third Edition.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Online notes: https://www.cisco.com/c/en_in/products/security/what-is-network-security.html
2. Online ppts: https://training.apnic.net/wp-content/uploads/sites/2/2016/12/TSEC01.pdf
3. NPTEL online video content: https://nptel.ac.in/courses/106105031

E-content:

1. Pawar, M. V., & Anuradha, J. (2015). Network security and types of attacks in network. *Procedia Computer Science*, *48*, 503-506. https://www.sciencedirect.com/science/article/pii/S1877050915006353

2. Feng, G., Zhang, C., Si, Y., & Lang, L. (2020, July). An Encryption and Decryption Algorithm Based on Random Dynamic Hash and Bits Scrambling. In *2020 International Conference on Communications, Information System and Computer Engineering (CISCE)* (pp. 317-320). IEEE. https://ieeexplore.ieee.org/document/9258781

3. S. Yuan and D. Stewart, "Protection of Optical Networks against Interchannel Eavesdropping and Jamming Attacks," *2014 International Conference on Computational Science and Computational Intelligence*, 2014, pp. 34-38, doi: 10.1109/CSCI.2014.14. https://ieeexplore.ieee.org/document/6822080

4. Yi Qian; Feng Ye; Hsiao-Hwa Chen, "Cryptographic Techniques," in Security in Wireless Communication Networks , IEEE, 2022, pp.51-76, doi: 10.1002/9781119244400.ch4. https://ieeexplore.ieee.org/document/9635156

Topics relevant to "EMPLOYABILITY SKILLS": Encryption techniques, Security system, Network security with applications, Cyber Security, System Security for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. T. Prabhu
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE5016	Course Title: IC Fabrication Technology Type of Course: Theory only		L-T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	VLSI Design, design and implementation of VLSI circuits for complex digital and analog systems, NMOS and CMOS fabrication steps, design for testability and design verification.					
Anti-requisites	NIL					
Course Description	The purpose of this course is to enable the students to understand the basics of IC fabrication technology. This course aims to foster knowledge of Integrated circuit technology and fabrication techniques. This course introduces the various manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI chip fabrication and Microcontrollers. This course also discusses the complexities and challenges associated with VLSI chip fabrication and different Microcontrollers. The course gives clear understanding about entire Chip fabrication.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of IC fabrication technology and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: 1. Describe the process involved in semiconductor crystal growth and fabrication. 2. Classify various lithography and etching techniques used for pattern transfer. 3. Summarize the diffusion and ion implantation mechanisms in IC fabrication. 4. Discuss the process involved in packaging and yield.					
Course Content:						
Module 1	Crystal Growth	Quiz	Memory Recall based Quizzes	10 Session		
Topics: Introduction, electronic-grade silicon, czochralski crystal growing-crystal structure, crystal growing theory, crystal growing practise, shaping operations, etching, process considerations.						
Module 2	Oxidation and lithography	Assignment	Theoretical Understanding	10 Session		
Topics: Growth mechanics and kinetics, thin oxides, oxidation techniques and systems, optical lithography-optical resists, electron lithography-resists, mask generation, X-ray lithography-resists, ion lithography						
Module 3	Diffusion and Implantation	Assignment	Theoretical Understanding	10 Session		

Topics:

Models of diffusion in solids, one dimensional diffusion equations, atomic diffusion mechanisms, measurement techniques, Ion implantation-range theory-ion stopping, range distribution, Furnace Annealing, high energy implantation.

Module 4	Packaging, Yields, Processing Facility Setup and Silicon Foundries	Assignment	Theoretical Understanding	10 Session

Topics:

Testing, dicing of wafers, packaging, bonding, yield theory and measurements. Measurement techniques: Optical microscope, Scanning Electron Microscope, energy dispersive analysis of X-rays, Augue analysis, Secondary Ion Mass Spectroscopy (SIMS), Laser Ion Mass Spectroscopy (LIMS), Rutherford Backscatter Spectroscopy (RBS), Silicon Foundries

List of Laboratory Tasks: Nil

Targeted Application & Tools that can be used:

Application Area – Facility Manager, Process Engineer , Process development designer , Facility Engineer, Process simulation Engineer.

Professionally Used Software: ATHENA/SILVACO , SYNOPSIS , TCAD , VISUAL TCAD

Project work/Assignment:

1. Article review: At the end of course an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link .

2. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

3. Project Assignment:- Implementation of various concepts in from deep learning using TCAD and SILVACO

Text Book

1. S.M. Sze, "VLSI technology", Tata McGraw Hill, Second Edition, 2017.

Reference(s):

Reference Books

1. S. K. Ghandhi, "VLSI Fabrication Principles: Silicon and Gallium Arsenide", John Wiley and Sons Inc., New York , 1983.
2. Plummer J. D., Deal M. D. and P. B. Griffin , "Silicon VLSI Technology: Fundamentals, Practice and Modeling" , Pearson/PHI, 2001.
3. Plummer J. D., Deal M. D. and P. B. Griffin , "Silicon VLSI Technology: Fundamentals, Practice and Modeling" , Pearson/PHI, 2001.
4. James Plummer, M. Deal and P.Griffin, "Silicon VLSI Technology", Prentice Hall, Electronics and vLSI series, 2000.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL - https://onlinecourses.nptel.ac.in/noc21_mm26/preview
2. Udemy - https://www.udemy.com/course/pcb-design-and-fabrication-for-everyone/
3. Coursera - https://www.coursera.org/lecture/leds-semiconductor-lasers/introduction-to-semiconductor-fundamentals-3zejs

E-content:

1. William Cheng-Yu Ma;Yan-Jia Huang;Po-Jen Chen;Jhe-Wei Jhu;Yan-Shiuan Chang;Ting-Hsuan Chang ,"Impacts of Vertically Stacked Monolithic 3D-IC Process on Characteristics of Underlying Thin-Film Transistor" , IEEE Journal of the Electron Devices Society 2020 , https://ieeexplore.ieee.org/document/9141258
2. NEGIN ZARAEE 1 , BOYOU ZHOU 1 , KYLE VIGIL 2 , MOHAMMAD M. SHAHJAMALI 3 , AJAY JOSHI 1 , AND M. SELIM ÜNLÜ , "Gate-Level Validation of Integrated Circuits With Structured-Illumination Read-Out of Embedded Optical Signatures" , IEEE,2020, https://ieeexplore.ieee.org/document/9063443
3. IN-GON LEE1 , WON-SEOK OH2 , YOON JAE KIM2 , AND IC-PYO HONG , "Design and Fabrication of Absorptive/ Transmissive Radome Based on Lumped Elements Composed of Hybrid Composite Materials" , IEEE Access 2020 , https://ieeexplore.ieee.org/document/9141287

Topics relevant to "EMPLOYABILITY SKILLS": " : IC Fabrication techniques and procedures, IC Assembling and Packing, Metallization applications, choices, physical vapour deposition, metallization problems, introduction to packaging, package types, packaging design considerations for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Mrs. Anupama Sindgi
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE5017	Course Title: Software Defined Radio Type of Course: Theory only	L- T-P- C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Wireless Communications					
Anti-requisites	NIL					
Course Description	The purpose of this course is to introduce the basic concepts of software-defined radio (SDR) with architectures and benefits. It is an inherent part of modern communication systems, where many processes, which used to be implemented in hardware, are defined in the software domain for flexibility and configurability. This course describes various components of software-defined-radios with the understanding of their limitation and applications.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of software defined radio and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.					
	On successful completion of this course the students shall be able to: 1. Understand the basic requirements, benefits and different models for Software Defined Radio. 2. Analyze the RF receiver for performance optimization. 3. Apply the complete knowledge of different blocks and techniques for Base Stations and Handsets.					
Course Content:						
Module 1	Introduction and Architecture of SDR	Assignment/ Quiz	Memory Recall based Quizzes	15 Sessions		
Topics: Requirement for Software defined radio, Benefits of multi-standard terminals, Operational requirements, models for SDR, Business Models for SDR, New Base-Station and Network Architectures, Smart antenna systems, Software defined radio architectures, Hardware specifications, Digital aspects of Software defined radio, Current technology limitations, Impact of Superconducting Technologies on Future SDR systems.						
Module 2	Flexible RF Receiver Architectures	Assignment/ Quiz	Real time Application Project	15 Sessions		
Topics: Receiver Architecture options, Implementation of a Digital Receiver, Influence of Phase Noise on EVM for Linear Transceiver, Multi-band Flexible Receiver Design, Problem of the Diplexer, Achieving Image Rejection, Dynamic Range Enhancement.						
Module 3	Flexible Transmitters and PAs	Assignment/ Quiz	Memory Recall based Quizzes	10 Sessions		
Introduction, Differences in PA Requirements for Base Stations and Handsets, Linear Upconversion Architectures, Constant-Envelope Upconversion Architectures, Broadband Quadrature Techniques.						
Targeted Application & Tools that can be used:						

These applications include the integration of wireless medical devices in a common communication platform for seamless interoperability, and cognitive radio (CR) for body area networks (BANs) and wireless sensor networks (WSNs) for medical environmental surveillance.

Professionally Used Software: GNU Radio, MATLAB

Project Work/Assignment:

1. Article review: At the end of course an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link .

3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

4. Project Assignments: Implementation of different blocks and various techniques for Software Defined Radio using MATLAB.

Text Book(s):

1. P Kenington, "*RF and Baseband Techniques for Software Defined Radio*", Artec House, 2005

Reference(s):

Reference Book(s):

1. Jeffrey Hugh Reed, "*Software Radio: A Modern Approach to Radio Engineering*", Prentice Hall Professional, 2002.
2. Tony J Rouphael, "*RF and DSP for SDR*," Elsevier Newnes Press, 2008.
3. Paul Burns, "*Software Defined Radio for 3G*," Artech House, 2002.

Online Resources (e-books, notes, ppts, video lectures etc.):

NPTEL Online Video Content: https://nptel.ac.in/courses/108107107

2. Online notes: https://www.electronics-notes.com/articles/radio/sdr-software-defined-radio-receiver/sdr-basics.php
3. Online ppts: https://www.powershow.com/view/3e8ba4-OGQ0N/Software_Defined_Radio_powerpoint_ppt_presentation
4. Online e-book: https://www.analog.com/en/education/education-library/software-defined-radio-for-engineers.html

E-content:

1. H. Zargariasl, P. Šolić, K. Radoš, T. Perković, Z. Blažević and J. J. P. C. Rodrigues, "Comparing RFID Tags Performance through Software Defined Radio," 2019 IEEE International Conference on RFID Technology and Applications (RFID-TA), 2019, pp. 494-498, doi: 10.1109/RFID-TA.2019.8892147. https://ieeexplore.ieee.org/document/8892147

2. T. -H. Nguyen and M. Yoo, "A behavior-based mobile malware detection model in software-defined networking," 2017 International Conference on Information Science

and Communications Technologies (ICISCT), 2017, pp. 1-3, doi: 10.1109/ICISCT.2017.8188590.
https://ieeexplore.ieee.org/document/8188590

3. N. Hosseini and D. W. Matolak, "Software defined radios as cognitive relays for satellite ground stations incurring terrestrial interference," 2017 Cognitive Communications for Aerospace Applications Workshop (CCAA), 2017, pp. 1-4, doi: 10.1109/CCAAW.2017.8001874.
https://ieeexplore.ieee.org/document/8001874

4. J. Pawlan, "An introduction to Software Defined Radio," 2015 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS), 2015, pp. 1-1, doi: 10.1109/COMCAS.2015.7360430.
https://ieeexplore.ieee.org/document/7360430

Topics relevant to "EMPLOYABILITY SKILLS": Software Defined Radio Architectures, Smart Antenna, Cognitive Radio and Flexible Transmitter, Ethical considerations while developing Software Defined Radio products for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. T. Prabhu
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE5018	Course Title: Memory Design Type of Course: Theory only	L-T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Basic concepts of simple circuit design involving diode and Transistor, their interconnections and current and voltage levels. Basics of logic gates and implementation of Digital Logic Circuits using gates, flip-flops, registers, multiplexers, decoders etc.					
Anti-requisites	NIL					
Course Description	The course aims at explaining the basics of memory and its architecture. This course insight into the detailed structure of SRAMs and DRAMs. The course thrusts on the modeling of the memory fault and advanced memory testing patterns. The course elaborates the reliability and radiation effect issues of semiconductor memories. Also the course discusses the high performance memory subsystems, advanced memory technologies and contemporary issues in real time.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of memory design and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: CO1 – Summarize the basic concepts of memories and its architecture. CO2 – Distinguish the application specific Volatile and Non Volatile Memories. CO3 – Apply the advanced technologies in the design of real memories. CO4 – Analyze the features of testability in advanced memories.					
Course Content:						
Module 1	Volatile Memories	Quiz	Comprehension	11 session		
Topics: Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs. DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.						
Module 2	Non-Volatile Memories	Assignment / Quiz	Application	11 session		
Topics: Non-Volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.						
Module 3	Advanced Memory Design	Assignment	Analysis	11 session		
Topics: Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory						

Devices.				
Module 4	High-Density Memory Packages	Project	Application	9 session

Topics: Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

Project Work/Assignment:

1. Case Studies: At the end of the course students will be given case study on "3D Memory design in VLSI". Students will be submitting a report in appropriate format.

2. Presentation: Individual presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

3. Project Assignment: The project work will be given on "Application Specific Volatile and Non-Volatile Memory" and the students have to complete the work using the Cadence tools and documentation of the entire work in prescribed format to be submitted.

Assignment 1: High Density Memory Packaging Technologies.

Assignment 2: Differentiate between the Volatile and Non-Volatile Memories

Text Book(s):

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience , 1st Edition, 2002
2. Kiyoo Itoh, "VLSI memory chip design", Springer International Edition, 2012

Reference(s):

Reference Book(s):

1. Takayuki Kawahara, Hiroyuki Mizuno," Green Computing with Emerging Memory: Low-Power Computation for Social Innovation", 1st Edition, Springer, 2012.
2. Ashok K Sharma, "Semiconductor Memories: Technology, Testing and Reliability", 2nd Edition, PHI, 1997
3. Hai Li, "Nonvolatile Memory Design: Magnetic, Resistive and Phase Change",1st Edition, CRC Press, 2011

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL Course on "Digital Computer Organization", by Prof. Dr. S K Lahiri, IIT KGP https://nptel.ac.in/courses/117105078
2. NPTEL Course on "Computer Architecture", by Prof. Smruti Ranjan Sarangi, IIT Delhi, https://onlinecourses.nptel.ac.in/noc22_cs15/preview /
3. NPTEL Course on "Computer architecture and organization" by By Prof. Indranil Sengupta, Prof. Kamalika Datta IIT Kharagpur, https://onlinecourses.nptel.ac.in/noc20_cs64/preview

E-content:

1. Samuel Spetalnick, Arijit Raychowdhury, "A Practical Design-Space Analysis of Compute-in-Memory With SRAM", IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: 69, Issue: 4, April 2022, pp: 1466 - 1479, DOI: 10.1109/TCSI.2021.3138057, https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9674198
2. Chao Wang, Zhaohao Wang, Gefei Wang, Youguang Zhang, Weisheng Zhao, "Design of an Area-Efficient Computing in Memory Platform Based on STT-MRAM", IEEE Transactions on Magnetics, Volume: 57, Issue: 2, Feb. 2021, DOI: 10.1109/TMAG.2020.3016741, https://ieeexplore.ieee.org/document/9167274

3. Yinjin Fu, Yutong Lu, Zhiguang Chen, Yang Wu, Nong Xiao, "Design and Simulation of Content-Aware Hybrid DRAM-PCM Memory System", IEEE Transactions on Parallel and Distributed Systems, Volume: 33, Issue: 7, July 1 2022, pp:1666 - 1677, DOI: 10.1109/TPDS.2021.3123539, https://ieeexplore.ieee.org/document/9591354 4. Andrea Ceschini, Antonello Rosato, Massimo Panella, "Design of an LSTM Cell on a Quantum Hardware", IEEE Transactions on Circuits and Systems II: Express Briefs, Volume: 69, Issue: 3, March 2022, pp: 1822 - 1826, DOI: 10.1109/TCSII.2021.3126204 https://ieeexplore.ieee.org/document/9606223
Topics relevant to "EMPLOYABILITY SKILLS": SRAM, DRAM and its architecture, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices, Memory Hybrids (2D & 3D), Memory Stacks for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. Joseph Anthony Prathap,
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE6003	Course Title: LOW POWER VLSI DESIGN Type of Course: Theory only	L- T-P- C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Basic concepts of digital circuits like gates, flip-flops, registers, multiplexers, decoders etc. Fundamentals of Analog and Digital VLSI design. HDL Languages like Verilog / VHDL.					
Anti-requisites	NIL					
Course Description	The purpose of this course is to enable the students to appreciate the fundamentals of low power architectures and systems. The course is both conceptual and analytical in nature and needs fair knowledge of VLSI design. The course also helps to develop a broad insight into the methods used to confront the low power issue from circuit level to system level of abstraction. It also enhances student's abilities to develop a low power design architecture and analyze various parameters.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of low power VLSI design and attain EMPLOYABILITY SKILLS by using PROBLEM SOLVING.					
Course Outcomes	On successful completion of this course the students shall be able to: 1. Identify the sources of power dissipation in CMOS integrated circuits. 2. Illustrate the different approaches of Low power design at circuit level. 3. Summarize issues in Low Power Design at circuit and logic levels. 4. Explain leakage sources and reduction techniques.					
Course Content:						
Module 1	Device & Technology Impact on Low Power	Assignment	Designing and Analysis task	10 Sessions		
Topics: Introduction: Sources of Power dissipation: Dynamic Power Dissipation, Short Circuit Power, Switching Power Glitching Power. Emerging Low power approaches, Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation., Static Power Dissipation, Degrees of Freedom, Supply Voltage Scaling Approaches: Device feature size scaling, Multi-Vdd Circuits						
Module 2	Power analysis	Assignment	Simulation and analysis task	10 Sessions		
Topics: Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation, Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.						
Module 3	Low Power Design at circuit and logic level	Assignment	Design Analysis	10 Sessions		

Topics:

Low Power Design Circuit Level: Transistor and gate sizing, network restructuring and Reorganization. Special Flip Flops & Latches design, high capacitance nodes, low power digital cells library.

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Module 4	Leakage Power minimization Approaches, Adiabatic switching, Memory Design	Assignment/Project	Data Analysis	10 Sessions

Topics: Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components. Variable-threshold-voltage CMOS (VTCMOS) approach, Multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Low power Clock Distribution, CAD tools for low power synthesis, Special Techniques: Power Reduction in Clock networks, CMOS Floating Node, Low Power Bus Delay balancing, and Low Power Techniques for SRAM.

Targeted Application & Tools that can be used:

Application Area is high-performance digital systems, such as microprocessors, digital signal processors (DSPs).

Professionally Used Software: Xilinx-ISE; VIVADO; Cadence-Virtuoso.

Open source tools: EDA Playground; LT-Spice; Microwind.

Project work/Assignment:

1. Case Studies: At the end of the course students will be given a topic related to Low Power VLSI Design that would have been published, as a case study. Students will be submitting a report in appropriate format.

2. Book/Article review: At the end of each module a book reference or an article topic will be given to each student. They need to visit the library and write a report on their understanding about the assigned article in appropriate format.

3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

4. Assignments:

Project 1. Design a cyclic redundancy Checker using Verilog. Compare the power and area consumption for the code using two different approaches. Design and implement in Xilinx-VIVADO. Also perform debugging using the available tools.

Project 2. Design a low power and highly efficient 8-bit processor using Xilinx Vivado tool and Compare the power consumption with existing codes.

Assignment 1: Design a 4x4 NOR ROM with the following row content: Row[0] = 1011, Row[1] = 0110, Row[2] = 1010 and Row[3] = 1111.

Assignment 2: Sketch a transistor-level schematic of a CMOS complex logic gate that realizes (a) the function and (b) draw stick diagram of the same complex logic gate.

Textbook(s):

1. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI circuit design", John Wiley & Sons Inc., 1st edition, 2000.

References:

Reference Book(s):

2. Soudris, Dimitrios, Christrian Pignet, Goutis, Costas, "Designing CMOS circuits for low power," Springer International, 2004. (1st Edition)
3. Ajit Pal, —Low-Power VLSI Circuits and Systems‖, Springer, 2015. (1st Edition)
4. A. P. Chandrakasan, R.W. Broderson, "Low Power Digital VLSI Design", IEEE Press, 1998. (1st Edition)
5. Gary K.Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 1998. (1st Edition)
6. Jan M. Rabaey, Massoud Pedram, "Low power Design methodologies", Kluwer Academic Press, 1996. (1st Edition)
7. Michael Keating, David Flynn "Low Power Methodology Manual for System-On-Chip Design" Springer Publication 2007. (1st Edition)

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Lecture videos for Low Power VLSI Circuits & Systems by Prof. Ajit Pal Department of Computer Science and Engineering, IIT Kharagpur – NPTEL https://nptel.ac.in/courses/106/105/106105034/
2. PPT on Low Power VLSI Design, Link : https://nijwmwary.com/low-power-vlsi-circuits-systems/

E-content:

1. Shanbhag, Naresh R. "Algorithms transformation techniques for low-power wireless VLSI systems design." *International Journal of Wireless Information Networks* 5, no. 2 (1998): 147-171. https://link.springer.com/article/10.1023/A:1018869519651
2. Gopalaiah, S. V., A. P. Shivaprasad, and Sukanta K. Panigrahi. "Design of low voltage low power CMOS OP-AMPS with rail-to-rail input/output swing." In *17th International Conference on VLSI Design. Proceedings.*, pp. 57-61. IEEE, 2004. https://ieeexplore.ieee.org/document/1260903
3. R. Raut and O. Ghasemi, "A power efficient wide band trans-impedance amplifier in sub-micron CMOS integrated circuit technology," *2008 Joint 6th International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference*, 2008, pp. 113-116, doi: 10.1109/NEWCAS.2008.4606334. https://ieeexplore.ieee.org/document/4606334
4. Badawy, Wael, and Magdy Bayoumi. "Low power VLSI architecture for 2D-mesh video object motion tracking." In *Proceedings IEEE Computer Society Workshop on VLSI 2000. System Design for a System-on-Chip Era*, pp. 67-72. IEEE, 2000. https://ieeexplore.ieee.org/abstract/document/844532

Topics relevant to "EMPLOYABILITY SKILLS": SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. Ashutosh Anand
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE6004	Course Title: Processor Design Type of Course: Theory only		L-T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Basic concepts of Digital design involving Combinational and Sequential design. Basics of Digital System Design and its real time implementation using the FPGA devices.					
Anti-requisites	NIL					
Course Description	This course is about designing modern pipelined RISC processor. This Course revisits the synchronization and pipelining concepts taught in prerequisites. Then the course extends the timing analysis done in prerequisite courses. After that the design of a simple multi-cycle processor is introduced. This is followed by the detailed design of a single cycle processor. Then the design of pipeline of RISC CPU is handled. Advanced topics like resolving dependencies by compiler and hardware is handled. Then students are sensitized to multiple instruction issue. Finally BUS design is introduced. For this, basic introduction to BUS is given followed by AMBA bus is discussed, with the design of Bus interface and Bus bridges.						
Course Objective	The objective of the course is to familiarize the learners with the concepts of processor design and attain EMPLOYABILITY SKILLS by using PARTICIPATIVE LEARNING.						
Course Outcomes	On successful completion of this course the students shall be able to: CO1 - Demonstrate the processor and its specifications such as Multi-cycle, Single-cycle and pipelined CPU. CO2 - Develop the bus interface and peripheral devices compatible to bus for the development of the processor. CO3 - Analyze the timing issues in the Processor design. CO4 - Analyze the issues in data dependencies by stalling, data forwarding and bypassing						
Course Content:							
Module 1	Synchronization and Pipelining Concepts	Quiz	Memory Recall based Quizzes	9 session			
Topics: Introduction: Basic Processor Architecture, Instruction Set Design, Data-path and Controller, Timing, Pipelining.							
Module 2	CISC Processor Design	Assignment / Quiz	Application level activities	11 session			
Topics: CISC Processor Design: Architecture, hardware flowchart, implementing from flowchart, exception, control store, microcode design.							

Module 3	RISC Processor Design	Assignment	Application level activities	13 session
Topics: Single cycle implementation, multi cycle implementation, pipelined implementation, exception and hazards handling, Superscalar organization, superscalar pipeline overview, VLSI implementation of dynamic pipelines, register renaming, reservation station, re-ordering buffers, branch predictor, and dynamic instruction scheduler.				
Module 4	Bus in Processor	Project	Analysis and Application	9 session
Topics: Bus Topologies, AMBA Bus, Bus Interface and Bridge Design, Bus Function Models, Network-on-Chip				

Project Work/Assignment:

1. Book/Article review: At the end of each module a book reference or an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. https://puniversity.informaticsglobal.com/login will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

2. Project Assignment: The project work will be given on "Design of Advanced Versatile Processor using FPGA" and the students have to complete the work using the Cadence tools and documentation of the entire work in prescribed format to be submitted

Assignment 1: A design method of pipelined RISC processor and its implementation. An algorithm written in C is compiled and assembly code is produced, this code is tested on the implemented design on an FPGA Board

Assignment 2: Trends in RISC and CISC processor applications

Text Book(s):

1. David A. Patterson, John L. Hennessy, "Computer Organization and Design: The Hardware/Software Interface, The Morgan Kaufmann Series in Computer Architecture and Design, 4th Edition, 2011,

John P. Shen, "Modern Processor Design: Fundamentals of Superscalar Processors", 2nd Edition, McGraw-Hill Series in Electrical and Computer Engineering , 2013

Reference(s):

Reference Book(s):

1. Ron Sass, Andrew G Schmidt, "Embedded Systems Design with Platform FPGAs Principles and Practices", 2011, First Edition, Tata McGraw Hill, India.
2. Wayne Wolf, "FPGA Based System Design", 2011, First Edition, Prentices Hall Modern Semiconductor Design Series, USA.
3. Charles H Roth. Jr "Digital Systems design using VHDL", 2012, 2nd Edition, PWS publishing company (Thomson Books), USA.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL Course on Embedded System Design with ARM, Prof. Indranil Sengupta, Prof. Kamalika Datta, IIT Kharagpur, https://nptel.ac.in/courses/106105193
2. NPTEL Course on Computer Architecture(Course sponsored by Aricent), Prof.Madhu Mutyam, IIT Madras, https://nptel.ac.in/courses/106106134
3. NPTEL Course on Advanced Computer Architecture, Prof. John Jose, IIT Guwahati, https://nptel.ac.in/courses/106103206

E-content:

1. Daniel Valencia , Saeed Fouladi Fard, and Amir Alimohammad, "An Artificial Neural Network Processor With a Custom Instruction Set Architecture for Embedded Applications", IEEE Transactions On Circuits and Systems—I: Regular Papers, Vol. 67, No. 12, December 2020, pp:5200-5210. https://ieeexplore.ieee.org/document/9126204
2. Pietro Nannipieri , Stefano Di Matteo, Luca Baldanzi, Luca Crocetti , Luca Zulberti, Sergio Saponara, and Luca Fanucci, "VLSI Design of Advanced-Features AES Cryptoprocessor in the Framework of the European Processor Initiative", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 30, No. 2, February 2022, pp: 177-186. https://ieeexplore.ieee.org/document/9631958
3. Chen-Chien Kao, Chiao-En Chen, and Chia-Hsiang Yang, "Hybrid Precoding Baseband Processor for 64 × 64 Millimeter Wave MIMO Systems", IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 69, No. 4, April 2022, pp: 1765-1773. https://ieeexplore.ieee.org/document/9667330

Mohammad Rahmani Fadiheh, Alex Wezel, Johannes Muller, Jorg Bormann, Sayak Ray, Jason M. Fung, Subhasish Mitra, Dominik Stoffel, Wolfgang Kunz, "An Exhaustive Approach to Detecting Transient Execution Side Channels in RTL Designs of Processors", IEEE Transactions on Computers, 2022 https://ieeexplore.ieee.org/document/9716812

Topics relevant to "EMPLOYABILITY SKILLS": CISC Processor Design: Architecture, hardware flowchart, implementing from flowchart, exception, control store, microcode design, Bus Interface and Bridge Design, Bus Function Models, Network-on-Chip for developing Employability Skills through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. Joseph Anthony Prathap,
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE6005	Course Title: Embedded Intelligence Type of Course: Theory only	L-T- P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Knowledge of C or Python Language, Knowledge of stm32.					
Anti-requisites	NIL					
Course Description	Nowadays, you may have heard of many keywords like Embedded AI /Embedded ML /Edge AI, the meaning behind them is the same, I.e. To make an AI algorithm or model run on embedded devices. Due to a massive gap between both technologies, techies don't know where to start with it. So we thought to share our engineer's experience with you via this course. We have created an application to recognize the fault of a motor based on the vibration pattern. An Edge AI node developed to perform the analysis on the data captured from the accelerometer sensor to recognize the fault. We have created detailed videos with animation to give our students an engaging experience while learning this stunning technology. We assure you will love this course after getting this hands-on experience.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of embedded intelligence and attain EMPLOYABILITY SKILLS by using PROBLEM SOLVING.					
Course Outcomes	On successful completion of the course the students shall be able to: 1. get conceptual and practical clarity on Embedded AI 2. build similar kind of applications in Embedded AI 3. get Python scripts and C code(stm32) for Data capturing, Data Labeling and Inference.					
Course Content:						
Module 1	Image Classification	Assignment	Memory Recall based Quizzes	13 *Sessions*		
Topics: The concept of computer vision and how it can be used to solve problems. How digital images are created and stored on a computer. Neural networks and demonstration and classify simple images. train an image classifier and deploy it to an embedded system.						
Module 2	Convolutional Neural Networks	Assignment/mini project	Memory Recall based Quizzes	13 *Sessions*		
Topics: Basics of convolutional neural networks (CNNs) and how to create a more robust image classification model. Internal workings of CNNs (e.g. convolution and pooling) along with some visualization techniques used CNNs. concept of data augmentation to the training process. Train own CNN and deploy it to an embedded system.						
Module 3	Object Detection	Assignment/mini project	Programing / simulation	14 *Sessions*		

Topics: The basics of object detection and image classification. The math involved to measure objection detection performance. Introduction of several popular object detection models and demonstrate the process required to train such a model in Edge Impulse. Deploy an object detection model to an embedded system.				
List of Laboratory Tasks: Nil				
Targeted Application & Tools that can be used: Targeted Applications: This course is contributed for placement in data science companies, research & development work and also useful to know the existing & developing Artificial Intelligence. Professionally Used Software: MatLab, Phython				
Project work/Assignment:				
1. Article review: At the end of course an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link . 3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same. 4. Project Assignment: - Implementation of various concepts in from Embedded AI using Python/ MATLAB/ SCILAB				
Text Books: 1. Intelligence for Embedded Systems, A Methodological Approach. Cesare Alippi, Springer, 2014. ISBN: 978-3-319-05278-6 2. Intelligence for Embedded Systems: A Methodological Approach,2014th Edition. Springer ISBN-13: 978-3319052779. ISBN-10: 3319052772				
E-content: 1. Sara Anastasi, Marianna Madonna, Luigi Monica, Implications of embedded artificial intelligence - machine learning on safety of machinery, Procedia Computer Science, Volume 180, 2021, Pages 338-343, ISSN 1877-0509, https://doi.org/10.1016/j.procs.2021.01.171. 2. Anzhi Zhu, Application of artificial intelligence technology and embedded digital image in interior design, Microprocessors and Microsystems, Volume 81, 2021, 103782, ISSN 0141-9331. https://doi.org/10.1016/j.micpro.2020.103782. 3. Xiaonan Ding, Pengfei Shi, Xingming Li, Regional smart logistics economic development				

<table>
<tr><td colspan="2">based on artificial intelligence and embedded system, Microprocessors and Microsystems, Volume 81, 2021, 103725,

ISSN 0141-9331, https://doi.org/10.1016/j.micpro.2020.103725.

4. Nassim Abderrahmane, Edgar Lemaire, Benoît Miramond, Design Space Exploration of Hardware Spiking Neurons for Embedded Artificial Intelligence, Neural Networks, Volume 121, 2020, Pages 366-386,

ISSN 0893-6080, https://doi.org/10.1016/j.neunet.2019.09.024.</td></tr>
<tr><td colspan="2">Topics relevant to “EMPLOYABILITY SKILLS”: Computational intelligence algorithms, Data classification, Regression, Applications of Machine Learning in data analysis for developing Employability Skills through Problem Solving techniques. This is attained through assessment component mentioned in course handout.</td></tr>
<tr><td>Catalogue prepared by</td><td>Mr. G Tirumala Vasu</td></tr>
<tr><td>Recommended by the Board of Studies on</td><td>BOS NO: 15th BOS held on 28/07/2022</td></tr>
<tr><td>Date of Approval by the Academic Council</td><td>Academic Council Meeting No. 18th , Dated 03/08/2022</td></tr>
</table>

Course Code: ECE6006	Course Title: VLSI Signal Processing Type of Course: Theory only		L-T-P-C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Basic concepts of CMOS Analog and Digital design like gates, flip-flops, registers, multiplexers, decoders, OPAMP, Differential amplifier, LNA etc. HDL Languages like Verilog / VHDL. Fundamental understanding of the DSP, filters like IIR and FIR filters. Handson knowledge of MATLAB.					
Anti-requisites	NIL					
Course Description	The purpose of this course is to enable the students to appreciate the fundamentals VLSI Signal Processing. This course could be the bridge between the VLSI design and its interaction with the different signals. The course is both conceptual and analytical in nature and needs fair knowledge of VLSI design architecture along with the sound knowledge of DSP algorithm. The course also helps to develop a broad insight into the methods used to confront the issues related to the signal processing in different VLSI design from circuit level to system level of abstraction. It also enhances student's abilities to develop a different VLSI architecture DSP algorithm and analyze various parameters.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of VLSI signal processing and attain EMPLOYABILITY SKILLS by using PROBLEM SOLVING.					
Course Outcomes	On successful completion of this course the students shall be able to: 1. Familiarize with VLSI algorithms and architectures for DSP. 2. Explain the optimize design in terms of area, speed and power. 3. Incorporate pipeline-based architectures in the design. 4. Illustrate the HDL simulation of various DSP algorithms. 5. Implement the basic architectures for DSP using CAD tools					
Course Content:						
Module 1	Introduction to DSP	Quiz	Memory Recall based Quizzes	10 sessions		
Topics: Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.						
Module 2	Unfolding and Folding	Assignment / Quiz	Memory Recall based Quizzes /Programming and Simulation task	10 sessions		
Topics: Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.						
Module 3	Systolic Architecture Design	Quiz	Memory Recall based Quizzes	10 sessions		

Topics:

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays

Module 4	Fast Convolution	Assignment	Memory Recall based Quizzes /Programming and Simulation task	10 sessions

Topics

Fast Convolution: Introduction, Cook, Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection

Targeted Application & Tools that can be used:

Application: VLSI signal Processing is one of the hottest research topics in field mixed signal IC design. The students will be able to find career opportunities in various domains such as:

Digital Signal Processors (DSPs).

AMS (Analog Mixed Signal) designer.

AMS verification engineer.

Layout design engineer.

Physical design engineer.

DFT engineer.

Application engineer technical support.

Professionally Used Software: MATLAB, Simulink, Xilinx and Cadence.

Project Work/Assignment:

1. Case Studies: At the end of the course students will be given a topic related to VLSI Signal Processing that would have been published, as a case study. Students will be submitting a report in appropriate format.

2. Book/Article review: At the end of each module a book reference or an article topic will be given to each student. They need to visit the library and write a report on their understanding about the assigned article in appropriate format.

3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

Text Book(s):

1. Keshab K. Parhi. *VLSI Digital Signal Processing Systems*, Wiley-Inter Sciences, 1st Edition
1999

Reference(s):

Reference Book(s):

1. Mohammed Ismail, Terri, Fiez, *Analog VLSI Signal and Information Processing,* McGraw Hill, 1994 (1st Edition).
2. Kung. S.Y., H.J. While house T.Kailath, *VLSI and Modern singal processing*, Prentice Hall, 1985 (1st Edition).

3. Jose E. France, YannisTsividls, *Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing*' Prentice Hall, 1994 (1st Edition).
4. Medisetti V. K, "*VLSI Digital Signal Processing*", 1995, IEEE Press (NY), USA (1st Edition).

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL Video lectures on "VLSI Signal Processing" by Prof. Mrityunjoy Chakraborty, IIT KGP
https://onlinecourses.nptel.ac.in/noc20_ee44/preview

2. NPTEl Video lectures on "VLSI for Signal Processing" IIT Madras by Prof. Nitin Chandrachoodan https://www.youtube.com/playlist?list=PL3p-ZpXPqK6vvxeTp1k4kDMJj74WIetyC
3. PPT on VLSI signal processing. Link - https://slideplayer.com/slide/8341456/
4. PPT on VLSI Signal processing architecture, Link- https://slideplayer.com/slide/5270060/

E-content:

1. Vittoz, Eric A. "Analog VLSI signal processing: Why, where, and how?." *Analog Integrated Circuits and Signal Processing* 6, no. 1 (1994): 27-44. https://link.springer.com/article/10.1007/BF01250733
2. Darji, Anand D., Rajul Bansal, S. N. Merchant, and Arun N. Chandorkar. "High speed VLSI architecture for 2-D lifting Discrete Wavelet Transform." In *Proceedings of the 2011 Conference on Design & Architectures for Signal & Image Processing (DASIP)*, pp. 1-6. IEEE, 2011. https://ieeexplore.ieee.org/abstract/document/6136866
3. Caffarena, Gabriel, Olivier Sentieys, Daniel Menard, Juan A. López, and David Novo. "Quantization of VLSI digital signal processing systems." *EURASIP Journal on Advances in Signal Processing* 2012, no. 1 (2012): 1-2. https://link.springer.com/article/10.1186/1687-6180-2012-32
4. Bamford, Simeon A., Roni Hogri, Andrea Giovannucci, Aryeh H. Taub, Ivan Herreros, Paul FMJ Verschure, Matti Mintz, and Paolo Del Giudice. "A VLSI field-programmable mixed-signal array to perform neural signal processing and neural modeling in a prosthetic system." *IEEE transactions on neural systems and rehabilitation engineering* 20, no. 4 (2012): 455-467. https://ieeexplore.ieee.org/abstract/document/6177267

Topics relevant to "EMPLOYABILITY SKILLS VLSI Design, Mixed Signal VLSI Design, FIR and IIR filter application design, folding and unfolding for developing Employability Skills through Problem Solving techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. Ashutosh Anand
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

a. OPEN ELECTIVES

Course Code: ECE5001	Course Title: Wearable Computing Type of Course: Theory Only	L- T-P- C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	NIL					
Anti-requisites	NIL					
Course Description	This course provides insights into the fundamental concepts of wearable sensing, intelligent processing and actuating techniques related to wearable computing. The course emphasizes on the issues and constraints on energy harvesting requirements, communication technologies, development of body sensor nodes culminating into wireless health platforms and their deployment strategies. The course engages students in several thought provoking real-life case studies in the domains of affective state recognition, sports, wearable electronics, emergency and rescue operations as well as their interface with cloud computing, which in turn helps in designing and implementing wearable computing device or application.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of wearable computing and attain ENTREPRENEURSHIP SKILLS by using PARTICIPATIVE LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: Identify the attributes, components, requirements and challenges of Wearable Computing. ii. Select wearable sensors and signal processing techniques to meet low power design requirements. iii. Employ techniques for modeling context, emotion, activity and data mining for wearable devices. iv. Illustrate various future applications and associated issues.					
Course Content:						
Module 1	Fundamentals of Wearable Computing	Quiz	Memory Recall based Quizzes	10 Sessions		
Topics: Wearable Computing - Introduction, Attributes, Components; Communication Technologies; Challenges and Opportunities of Wearables; Social Aspects of Wearability – Innovation and Aesthetics, On-body Interaction; Wearable Haptics –Haptic devices and Tactile displays, Case Studies.						
Module 2	Sensors and Signal Processing for Wearable Systems	Assignment / Quiz	Programming and Simulation task	14 Sessions		
Topics:						

Wearable Biomechanical and Chemical Sensors - Inertial Sensors like Accelerometers and Gyroscopes; Biophysiological Signals and

Sensors – ECE, EMG, GSR, PPG etc.; Issues in On-node Signal Processing; Low power design requirements, Energy Harvesting and Scavenging for wearables. Commercial and Non-commercial Sensor Node Platforms; Case Studies.

Module 3	Wearable Algorithms and Research towards Miniaturization	Assignment	Memory Interfacing Task and Analysis	10 Sessions

Topics:

Modeling - Context, Emotion, Physical activity; Data Mining for wearable health applications, Developing Miniaturized Wearable Applications - E-Textiles; WBAN; Wearable Internet of Things (WIoT); Case Studies.

Module 4	Future Wearable Technologies	Assignment	System Design Task and Analysis	07 Sessions

Topics:

Digital Health; Disruptive & Soft Wearable Sensing; E-Skin Technologies; Wearable Computing in Education; Wearable for Industry 4.0; Data for life & Regulations; Case Studies.

Targeted Application & Tools that can be used:

Application Area:

This course will enable students to learn and understand social and industrial aspects of developing wearable devices. Sensing and processing using small and resource constrained devices, modeling techniques and their deployment issues on such portable devices will be discussed. Various mobile and wearable apps will give a quick start in this emerging field of application. This course will enable students to become a System Designer, Digital Health Expert and Real-world developer to name a few.

Professionally Used Software: Arduino and/or Raspberry Pi kits for initial prototyping / Android Studio / WearOS etc.

Project work/Assignment:

1. Case Studies: At the end of the course students will be given a 'real-world' application based system design case studies in the domains like sports, wearable electronics, emergency and rescue operations. Students will be submitting a report which will include Circuit Diagrams, Design, Working Mechanism and Results etc. in appropriate format.

2. Book/Article review: At the end of each module a book reference or an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. <https://presiuniv.knimbus.com/user#/home >.

3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

4. Project Assignment: Download an open source data sensed from mobile and wearable devices and apply various AI / machine learning algorithms in order to classify various tasks and or activities.

Assignment: 1] Identify various wearable sensors for sports activity monitoring, processing elements, actuators and list out the issues and constraints in the form of a report.

Assignment 2: Identify the components of wearable health monitoring device which uses the concepts of WIoT and list out various device connections. Indicate the working mechanisms by drawing a flow-chart.

Textbook(s):

Edward Sazonov, Michael R. Neuman, *"Wearable Sensors: Fundamentals, Implementation and Applications",* Academic Press/Elsevier.

References

Reference Book(s)

1. Giancarlo Fortino, Raffaele Gravina, and Stefano Galzarano, *"Wearable Computing: From Modeling to Implementation of Wearable Systems Based on Body Sensor Networks",* IEEE Press, 2018.

2. Annalisa Bonfiglio and Danilo De Rossi, *"Wearable Monitoring Systems",* Springer.

3. Claire Rowland, Elizabeth Goodman, Martin Chalier, Ann Light, Alfred Lui, *"Designing Connected Products: UX for the Consumer Internet of Things",* O'Reilly Media, Inc.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Alexander Nelson Course on Wearable & Ubiquitous Computing (Fall 2020). <https://ahnelson.uark.edu/courses/csce-4-5013-wearable-ubiquitous-computing-fall-2020/>
2. The Father of Wearable Computing | Steve Mann | TEDxUTSC <https://www.youtube.com/watch?v=Z9qiWqRPrcw>
3. Wearable Computing: the Next Generation of 'Borg. https://www.youtube.com/watch?v=_V2i_7oX8mw
4. Music & Wearable Computing for Health and Learning by WANG Ye <https://www.youtube.com/watch?v=4QYpK-8rmmY>.
5. International Symposium on Wearable Computer <https://iswc.net/iswc22/>.

E-content:

1. Starner, Thad. "Human-powered wearable computing." *IBM systems Journal*, vol. 35, no. 3.4, (1996), pp. 618-629.
http://wearcam.org/ieeecomputer/r2025printout_from_html.pdf

2. Mann, S., "Wearable computing: Toward humanistic intelligence." *IEEE Intelligent Systems*, vol. *16, no.* 3, (2001), pp.10-15.
http://n1nlf-1.eecg.toronto.edu/ieeeis_intro.pdf

3. Starner, Thad. "The challenges of wearable computing: Part 1." *IEEE Micro*, vol. 21, no. 4 (2001), pp. 44-52.
https://ieeexplore.ieee.org/abstract/document/946681

4. Starner, Thad. "The challenges of wearable computing: Part 2." *IEEE Micro*, vol. 21, no. 4, (2001), pp. 54-67.

https://ieeexplore.ieee.org/abstract/document/946683

5. Amft, Oliver, and Paul Lukowicz. "From backpacks to smartphones: Past, present, and future of wearable computers." *IEEE Pervasive Computing* 8, no. 3 (2009): 8-13. https://ieeexplore.ieee.org/abstract/document/5165554

6. Seneviratne, Suranga, Yining Hu, Tham Nguyen, Guohao Lan, Sara Khalifa, Kanchana Thilakarathna, Mahbub Hassan, and Aruna Seneviratne. "A survey of wearable devices and challenges." *IEEE Communications Surveys & Tutorials*, 19, no. 4 (2017): 2573-2620. https://ieeexplore.ieee.org/abstract/document/7993011

7. Yang, J., Zhou, J., Tao, G., Alrashoud, M., Al Mutib, K. N., & Al-Hammadi, M. (2019). Wearable 3.0: from smart clothing to wearable affective robot. IEEE Network, 33(6), 8-14. https://ieeexplore.ieee.org/abstract/document/8933553

8. Godfrey, A., Hetherington, V., Shum, H., Bonato, P., Lovell, N. H., & Stuart, S. (2018). From A to Z: Wearable technology explained. Maturitas, 113, 40-47. https://www.sciencedirect.com/science/article/pii/S0378512218302330

9. Ometov, A., Shubina, V., Klus, L., Skibińska, J., Saafi, S., Pascacio, P., ... & Lohan, E. S. (2021). A survey on wearable technology: History, state-of-the-art and current challenges. Computer Networks, 193, 108074. https://www.sciencedirect.com/science/article/pii/S1389128621001651

Topics relevant to "ENTREPRENEURSHIP SKILLS": Challenges and Opportunities of Wearables; Social Aspects of Wearability – Innovation and Aesthetics, On-body Interaction; Wearable Haptics –Haptic devices and Tactile displays, Wearable Biomechanical and Chemical Sensors, for developing ENTREPRENEURSHIP SKILLS through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. Rajiv Ranjan Singh
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE5002	Course Title: MEMS and Nanotechnology Type of Course: Theory only		L- T-P- C	3	0	0	3
Version No.	2.0					
Course Pre-requisites	Basic of Analog Electronics, Sensors, Actuators, Process Control					
Anti-requisites	NIL					
Course Description	The course deals with Micro electro mechanical systems (MEMS), devices and technologies. The course also discusses Micro-machining and microfabrication techniques, including planar thin- film processing, silicon etching, wafer bonding, photolithography, deposition and etching. The course also includes Transduction mechanisms and modelling in different energy domains. The course emphasizes on analysis of micro machined capacitive, piezo resistive and thermal sensors/actuators and applications.					
Course Objective	The objective of the course is to familiarize the learners with the concepts of MEMS and nanotechnologies attain ENTREPRENEURSHIP SKILLS by using PARTICIPATIVE LEARNING.					
Course Outcomes	On successful completion of this course the students shall be able to: i.Discuss Methods for Processing MEMS materials ii.Develop Characteristic techniques of micro system fabrication process ii.Demonstrate the concepts of Nano technology v.Illustrate nano materials and various nano measurements techniques v.Implement nano scale manufacturing					
Course Content:						
Module 1	Introduction and Fundamentals MEMS Device Physics	Assignment/ Quiz	Memory Recall based Quizzes	10 Sessions		
Topics: Introduction, MEMS Overview, Microfabrication of MEMS: Surface Micromachining, Bulk Micromachining, LIGA, micromachining of polymeric MEMS devices. Actuation: Electrostatic Actuation, Piezoelectric Actuation, Thermal Actuation, Magnetic Actuation, Mechanical Vibrations, The single degree of Freedom System, The many Degrees of freedom system, Microsensing for MEMS: Piezoresistive sensing, Capacitive sensing, Piezoelectric sensing, Resonant sensing, Surface Acoustic Wave sensors.						
Module 2	MEMS Materials and fabrication process Modelling	Assignment/ Quiz	Memory Recall based Quizzes	10 Sessions		
Topics: Metals, semiconductors, thin films for MEMS and their deposition techniques, materials for polymer MEMS. Solid modeling: Numerical Simulation of MEMS, Mechanical Simulation, Electrostatic Simulation.						
Module 3	MEMS Switches and RF	Assignment/ Quiz	Memory Recall based Quizzes	12 Sessions		

	Applications			

Topics:

Switch parameters, basics of switching, Switches for RF and microwave applications, actuation mechanisms for MEMS devices, dynamics of switch operation, MEMS switch design considerations, Microwave Considerations, Material Consideration, Mechanical Considerations modeling and evaluation.

MEMS based RF and Microwave circuits: RF Filters, Micro machined Phase shifters, and Micro machined antenna.

Module 4	MEMS Inductors and Capacitors	Assignment/ Quiz	Memory Recall based Quizzes	8 Sessions

Topics:

MEMS Inductors: self and mutual inductance, micro machined inductors, modelling and design issues of planar inductors, variable inductor and polymer based inductor. MEMS Capacitors: MEMS gap tuning capacitor, MEMS area tuning capacitor, Dielectric Tunable capacitors.

Targeted Application & Tools that can be used:

Applications in various fields such as biomedical, optical, wireless networks, aerospace, and consumer products

Tools: COMSOL Multiphysics, Ansys, CST, ADS

Project Work/Assignment:

1. Study of various sensors.

2. Book/Article review:

At the end of each module a book reference or an article topic will be given to each student. They need to visit the library and write a report on their understanding about the assigned article in appropriate format.

3. Presentation:

There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same.

Text Book(s):

T1: Tai-Ran Hsu, "MEMS and Microsystems: Design and Manufacture," McGraw-Hill, 1st edition, ISBN: 0072393912.

T2: RF MEMS: Theory, Design, and Technology, Gabriel M. Rebeiz, John Wiley & Sons, 1st edition, 2003.

Reference(s):

Reference Book(s):

R1 RF MEMS & Their Applications by Vijay K. Varadan, K. J. Vinoy and K. A. Jose John Wiley & Sons, 1st edition, 2003

R2 Introduction to Microelectromechanical Microwave Systems (2nd Edition) by Hector J.De Los Santos, Artech house, 2004.

R3 Mems Mechanical Sensors Microelectromechanical system series Srephen Beeby/Artech House, 1st edition 2004.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. NPTEL Video lectures on "MEMS and Microsystems" by Prof. Santiram Kal, IIT Kharagpur

https://nptel.ac.in/courses/117/105/117105082/

2. Video lectures on "Micro and Smart systems" by Prof. Sudip Misra", IISc Bangalore. https://nptel.ac.in/courses/112/108/112108092/

E-Content

1. Anand, Ashutosh, and Sudip Kundu. "Design of mems based piezoelectric energy harvester for pacemaker." In *2019 Devices for Integrated Circuit (DevIC)*, pp. 465-469. IEEE, 2019. https://ieeexplore.ieee.org/abstract/document/8783311
2. Anand, Ashutosh, Sourav Naval, Prasun Kumar Sinha, Nikhil Kumar Das, and Sudip Kundu. "Effects of coupling in piezoelectric multi-beam structure." *Microsystem Technologies* 26, no. 4 (2020): 1235-1252. https://link.springer.com/article/10.1007/s00542-019-04653-3
3. Hameed, Zohaib, and Kambiz Moez. "Design of impedance matching circuits for RF energy harvesting systems." *Microelectronics Journal* 62 (2017): 49-56. https://www.sciencedirect.com/science/article/pii/S0026269217301088
4. Abbaspour-Tamijani, Abbas, Laurent Dussopt, and Gabriel M. Rebeiz. "Miniature and tunable filters using MEMS capacitors." *IEEE Transactions on Microwave Theory and Techniques* 51, no. 7 (2003): 1878-1885. https://ieeexplore.ieee.org/abstract/document/1209276

Topics relevant to "ENTREPRENEURSHIP SKILLS": MEMS Inductors: self and mutual inductance, micromachined inductors, modelling and design issues of planar inductors, variable inductor and polymer based inductor. MEMS Capacitors: MEMS gap tuning capacitor, MEMS area tuning capacitor, Dielectric Tunable capacitors.for developing ENTREPRENEURSHIP SKILLS through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. Ashutosh Anand
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

<table>
<tr><td>Course Code:
ECE5003</td><td colspan="2">Course Title: Advanced Computer Networks
Type of Course: Theory Only</td><td>L- T-P- C</td><td>3</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>Version No.</td><td colspan="7">2.0</td></tr>
<tr><td>Course Pre-requisites</td><td colspan="7">NIL</td></tr>
<tr><td>Anti-requisites</td><td colspan="7"></td></tr>
<tr><td>Course Description</td><td colspan="7">The focus of this course will be to discuss OSI, TCP/IP and other networks models, Examples of Networks: Novell Networks, Arpanet, Internet, Network Topologies WAN, LAN, MAN. Physical Layer: Transmission media copper, twisted pair wireless, switching and encoding asynchronous communications; Narrow band, broad band ISDN and ATM; Data Link Layer: Design issues, framing, error detection and correction, CRC, Elementary Protocol-stop and wait, Sliding Window, Slip, Data link layer in HDLC, Internet, ATM; Medium Access Sub Layer: ALOHA, MAC addresses, Carrier sense multiple access, IEEE 802.X Standard Ethernet, wireless LANS, Bridges; Network Layer: Virtual circuit and Datagram subnets-Routing algorithm shortest path routing, Flooding, Hierarchical routing, Broad cast, Multi cast, distance vector routing; Dynamic Routing: Broadcast routing. Rotary for mobility, Congestion, Control Algorithms – General Principles of Congestion prevention policies. Internetworking: The Network layer in the internet and in the ATM Networks; Transport Layer: Transport Services, Connection management, TCP and UDP protocols; ATM AAL Layer Protocol; Application Layer: Network Security, Domain name system, SNMP, Electronic Mail; the World WEB, Multi Media.</td></tr>
<tr><td>Course Objective</td><td colspan="7">The objective of the course is to familiarize the learners with the concepts of advanced computer networks attain ENTREPRENEURSHIP SKILLS by using PARTICIPATIVE LEARNING.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">On successful completion of this course the students shall be able to:
1. Summarize the layers of OSI model, TCP/IP model associated with data communication and able to define its functions.
2. Employ different types of protocols associated with each layer of OSI model and multiple access techniques.
3. Demonstrate Ethernet based wired & wireless standards and different techniques for connecting networking devices for LANs, Virtual Networks & backbone networks.
4. Illustrate transport layer protocols and DNS protocols.</td></tr>
<tr><td>Course Content:</td><td colspan="7"></td></tr>
<tr><td>Module 1</td><td colspan="2">Layered tasks</td><td>Quiz</td><td colspan="2">Memory Recall based Quizzes</td><td>8 Sessions</td></tr>
<tr><td colspan="8">Topics:
OSI Model, TCP IP Suite, Hybrid Model, Jobs of layers. Network Models, Circuit switched networks</td></tr>
</table>

Module 2	DATA LINK CONTROL.	Assignment / Quiz	System Design Task and Analysis	12 Sessions
Topics: Framing, Flow and error control, Protocols, Noiseless channels and noisy channels HDLC MULTIPLE ACCESSE: MAC Sublayer Random access, Controlled access, Channelisation, wired and wireless protocols, Random access, ALOHA, CSMA, Controlled access				
Module 3	Connecting LANs.	Assignment	Memory Interfacing Task and Analysis	12 Sessions
Topics: Backbone LANs, Connecting devices, Back bone Networks, Virtual LANs Network Layer, Jobs, Ipv4 addresses, Ipv6 addresses, Transition from Ipv4 to Ipv6.				
Module 4	Transport layer	Assignment	System Design Task and Analysis	09 Sessions
Topics: Process to process Delivery, UDP, TCP, Comparison of UDP and TCP, Domain name system, Resolution, Transport protocols-UDP-user datagram, check sum, operation and uses, TCP-services, features, segment, TCP connection. Overview of Cryptography and IP Security				

Targeted Application & Tools that can be used:

Application Area:

Computer networking may be considered a branch of electrical engineering, telecommunications, computer science, information technology or computer engineering, since it relies upon the theoretical and practical application of the related disciplines.

A computer network facilitates interpersonal communications allowing users to communicate efficiently and easily via various means: email, instant messaging, chat rooms, telephone, video telephone calls, and video conferencing. Providing access to information on shared storage devices is an important feature of many networks. A network allows sharing of files, data, and other types of information giving authorized users the ability to access information stored on other computers on the network

Professionally Used Software: students can use open SOURCE Softwares like NS3 and Ubuntu.

Project work/Assignment:

1. Mini Projects: At the end of the course students will be assigned a project work on solving many societal relevant problems in the field of networking.

2. Book/Article review: At the end of each module a book reference or an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link .

3. Presentation: There will be a group presentation, where the students will be given a project on wearable device applications. They will have to explain/demonstrate the working and discuss the applications for the same.

Textbook(s):

Data Communication and Networking, B Forouzan, 5th Ed, TMH 2020.

References

Reference Book(s)

1. Computer Networks, James F. Kurose, Keith W. Ross: Pearson education, 2nd Edition, 2003.
2. Introduction to Data communication and Networking, Wayne Tomasi: Pearson education 2007.
3. Computer Networks, Tanenbaum

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Data Communication and Networking : B Forousan Fifth Edition < http://www.engppt.com/2009/12/networking-fourozan-ppt-slides.html >
2. Computer Networks 4th Edition Green Scissors < https://apiumhub.com/wp-content/uploads/formidable/10/data-communication-networking-forouzan-lecture-notes.pdf>

E-content:

1. Computer Communication Network https://doi.org/10.1186/1743-0003-9-21.2.
2. Communication Networks, IIT Kharagpur, Prof. Goutam Das https://nptel.ac.in/courses/117105148 .

Topics relevant to "ENTREPRENEURSHIP SKILLS: Framing, Flow and error control, Protocols, Noiseless channels and noisy channels HDLC MULTIPLE ACCESSE: MAC Sublayer Random access, Controlled access, Channelization, wired and wireless protocols for developing ENTREPRENEURSHIP SKILLS through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Dr. Divya Rani
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022

Course Code: ECE5004	Course Title: Pervasive computing Type of Course: Theory only		L-P-C	3	0	3
Version No.	2.0				
Course Pre-requisites	Pervasive computing is a combination of three technologies Micro electronic technology, digital communication and internet standardization, basic understanding of these technologies is essential.				
Anti-requisites	NIL				
Course Description	The purpose of this course is to provide an overview of pervasive computing technologies and its applications. This course highlights the device technology trends and protocols of pervasive computing. The course describes the challenges, opportunities, and devices that can be embedded into real time applications. It demonstrates the students to the design Speech Applications in Pervasive Computing. In this course the student will be able understand and apprehend the advanced real time computing applications.				
Course Objective	The objective of the course is to familiarize the learners with the concepts of pervasive computing attain ENTREPRENEURSHIP SKILLS by using PARTICIPATIVE LEARNING.				
Course Outcomes	On successful completion of this course the students shall be able to: 1) Demonstrate the concepts of pervasive computing and its applications. 2) Apply the knowledge of pervasive computing for web-based applications. 3) Develop the voice enabled and coding applications using pervasive computing 4) Analise the performance of pervasive computing-based device technologies and speech application				
Course Content:					
Module 1	Introduction to Pervasive Computing and its Applications	Quiz	Memory Recall based Quizzes	11 session	
Topics: Introduction to Pervasive Computing and its applications: Pervasive Computing, Applications, pervasive Computing devices and Interfaces, device technology trends, connecting issues and protocols, Application Examples of Pervasive Computing: Retail, Airline Check-in and booking, Sales force automation, Healthcare, Tracking, Challenges and future of Pervasive Computing.					
Module 2	Pervasive Computing and web based	Assignment / Quiz	Programming and Simulation task / Memory Recall based	12 session	

	Applications		Quizzes	
Topics: Pervasive Computing and web based Applications: - XML and its role in Pervasive Computing - Wireless Application Protocol (WAP) Architecture and Security - Wireless Mark-Up language (WML).				
Module 3	Device Technologies for Pervasive Computing	Assignment	Programming Assignment	17 session
Topics: Device Technologies for Pervasive computing : Hardware, Human-machine interfaces, Biometrics, Operating System, Device Connectivity Protocols, Security, Device Management, Web application concepts for pervasive computing, History, WWW architecture, Protocols, Trans-coding, Client Authentication via the Internet for pervasive computing				
Module 4	Speech Applications in Pervasive Computing	Assignment	Programming Assignment	17 session
Topics: Speech Applications in Pervasive Computing and security Voice Technology: Basics of Speech Recognition, Voice standards, Speech Applications, Speech and Pervasive Computing, Security.				
List of Laboratory Tasks: Nil				
Targeted Application & Tools that can be used: Targeted Applications: Data analytics, Computer Vision - Image & Video Processing, Speech Recognition, Automatic machine translation, object detection etc. Professionally Used Software: MATLAB				
Project Work/Assignment:				
1. Article review: At the end of course an article topic will be given to an individual or a group of students. They need to refer the library resources and write a report on their understanding about the assigned article in appropriate format. Presidency University Library Link . 3. Presentation: There will be a group presentation, where the students will be given a topic. They will have to explain/demonstrate the working and discuss the applications for the same. 4. Project Assignment:- Implementation of various concepts in from pervasive computing.				
Text Book(s): 1. Jochen Burkhardt, Dr..Horst Enn, Stefan Hepper, Klaus Rintdorff, Thomas Schack, Pervasive computing technology and architecture of mobile internet application"Published october 13, 2021. 2. Jochen Burkhardt, Horst Henn, Stefan Hepper, Thomas Schaec & Klaus Rindtorff: Pervasive Computing: Technology and Architecture of Mobile Internet Applications,				

Pearson Education, New Delhi, 2006.

Reference(s):

Reference Book(s):

1. Stefen Poslad: Ubiquitous Computing: Smart Devices, Environments and Interactions, Wiley, Student Edition, 2010.

2. A. Genco, S. Sorce: Pervasive Systems and Ubiquitous Computing, WIT Press, 2012.

3. Ajith Abraham (Ed.): Pervasive Computing, Springer-Verlag, 2012.

4. Guruduth S. Banavar, Norman H. Cohen, Chandra Narayanaswami: Pervasive Computing: An Application-Based Approach, Wiley Interscience, 2012.

5. Frank Adelstein, S K S Gupta, GG Richard & L Schwiebert: Fundamentals of Mobile and Pervasive Computing, Tata McGraw-Hill, New Delhi, 2000.

Online Resources (e-books, notes, ppts, video lectures etc.):

1. Free online self-paced course :-https://www.classcentral.com/course/wireless-communications-7503
2. Online notes :- https://www.iare.ac.in/sites/default/files/lecture_notes/IARE_WCN_NOTES.pdf
3. NPTEL online video content:- https://onlinecourses.nptel.ac.in/noc21_ee66/preview
4. Online ppts :- https://www.slideshare.net/manishreddy27/mobile-communication-72543084
5. Online ppts:- https://people.cs.georgetown.edu

E-content:

6. Vandana Dhingra; Anita Arora "Pervasive Computing: Paradigm for New Era Computing", in IEEE First International Conference on Emerging Trends in Engineering and Technology, vol.1, pp349- 359 2008. https://ieeexplore.ieee.org/document/4079026

7. Yenumula Venkataramana Reddy "Pervasive Computing: Implications, Opportunities and Challenges for the Society", in IEEE, Pervasive Computing: Implications, Opportunities and Challenges for the Society. Vol.1 2006. https://ieeexplore.ieee.org/abstract/document/4579923

8. Audrey Girouard, AndrewL. Kun, Anne Roudaut, Orit Shaer, "Pervasive computing Education" IEEE Pervasive Computing Volume: 17, Issue: 4, 01 Oct.-Dec. 2018. https://cil.csit.carleton.ca/b/wp-content/uploads/2019/02/PervasiveComputingEducation-2018.

9. Mahadev Satyanarayanan, Paramvir Bahl, Ramón Cáceres Nigel DaviesThe Case for VM-Based Cloudlets in Mobile Computing 01 -IEEE Pervasive Computing (IEEE)-Vol. 8, Iss: 4, pp 14-23 Oct 2009. https://typeset.io/papers/the-case-for-vm-based-cloudlets-in-mobile-computing-1rofse2vmh

Topics relevant to "ENTREPRENEURSHIP SKILLS : Pervasive Computing, Applications, pervasive Computing devices and Interfaces, device technology trends, connecting issues and protocols, Hardware, Human-machine interfaces, Biometrics, Operating System, Device Connectivity Protocols, Security, Device Management, Web application concepts for pervasive computing for developing ENTREPRENEURSHIP SKILLS through Participative Learning techniques. This is attained through assessment component mentioned in course handout.

Catalogue prepared by	Mrs. Manaswini R
Recommended by the Board of Studies on	BOS NO: 15th BOS held on 28/07/2022
Date of Approval by the Academic Council	Academic Council Meeting No. 18th , Dated 03/08/2022